i.MX8M Multimedia Workshop

Course Description

The i.MX8M family of application processors provide industry-leading video and audio processing for applications, that scale from consumer home audio to industrial building automation and mobile computers.
On this workshop we'll specifically target the i.MX8M with the following feature highlights:

- Video quality with full 4K UltraHD resolution and High Dynamic Range (HDR)
- Highest levels of pro audio fidelity
- Dual displays Up to 4Kp60 resolution on the HDMI 2.0a output and 1080p60 resolution on the MIPI-DSI (4-lanes) interface
- Graphical Processing Unit provides a 4-shader graphics core supporting the latest OpenGL ES 3.1, OpenCL 1.2, OpenGL 3.0, OpenVG and Vulkan standards
- Video processing unit Playback all the latest video standards up to 4K resolution using h.264, h.265 and VP9 (for YouTube 4K) codecs with HDR

This Workshop adopts a practical approach for learning the I.MX8M multimedia architecture and during the workshop, you'll take active part in several labs. We'll explore typical application use-cases, such as:

- Selecting the output display or displays, setting resolution and playing video content on each display or both
- Decode and stream 4K video file to HDMI display
- Face detection on a live video and stream it to two displays (via HDMI & MIPI-DSI)
- Filter applying on a live video stream and exploring performance while applying it on a CPU vs. GPU

As we go through the use-cases we'll delve into the underlying HW accelerators and get a deeper understanding of the architecture and its functionality.
This Workshop aims to provide you with an introduction with software tools/drivers on top of the Linux system to access and manipulate the multimedia accelerators.

During the practical labs you'll get familiar with Gstreamer, v4l2 and OpenCL and more.
By the end of this workshop you should have a good understanding of the Multimedia system, its capabilities and how it can be configured and manipulated. This should give you a head start when you develop your own iMX8M based product.

Course Duration

3 days

Goals

1. Become familiar with i.MX8M architecture
2. Become familiar with i.MX8M multimedia, graphics and audio capabilities
3. Understand in greater details all multimedia components
4. Efficiently use the software libraries and tools that allow controlling multimedia features
5. Be able to apply the theory to real life usage use cases

Target Audience

Software engineers that would like developing multimedia applications based on i.MX8M SoC.

Prerequisites

- i.MX8M architecture is recommended
- Experience in developing embedded systems
- C/C++ knowledge

Target platform

- Variscite DART-MX8M

Day 1

➢ i.MX8M Architecture Review

- i.MX8M block diagram
- i.MX8M key features
- Cortex-A53 CPU platform overview
- Cortex-M4 platform overview
- Memory system overview
- Clock, reset and power management
- Connectivity & mass storage overview
- Boot sequence

➢ i.MX8M Multimedia Overview

- Multimedia components
  - Enhanced LCD interface (eLCDIF)
  - GPU
  - HDMI Transmitter controller
  - MIPI_DSI
  - MIPI_CSI
  - Sony/Philips Digital Interface (SPDIF)
  - Synchronous Audio Interface (SAI)

➢ i.MX8M Display Controller Sub-System (DCSS)

- Display Controller Subsystem (DCSS)
  - DCSS major modes: HDR10, Dolby Vision
  - Pixel processing
  - Video only
  - Graphics only
  - Video with graphics overlay
  - Picture in graphics (PIG)
  - Picture in picture (PIP)
  - Video with PIP and graphics
  - DCSS memory map
  - Dolby Vision mode operation
  - HDR10 mode operation
  - DCSS interrupts
  - DCSS block control
  - Display timing generator
  - Context load
  - Graphics decompression
  - Decompression and tile to raster conversion
  - Display, prefetch and resolve
  - Scaler
  - Look up table load
  - HDR10 image processing
  - Color sub-sampler
  - Write scale and read surface

➢ i.MX8M Enhanced LCD Interface (eLCDIF)

- eLCDIF overview
- Bus master operation in write/display modes
- System bus master performance
- Write data path
- Read data path
- LCDIF interrupts
- LCDIF initialization
- MPU interface
- VSYNC interface
- CSI handshake interface
- Alpha blending interface
- DVI interface

❖ **Lab #1: Board Bring-Up and Development Environment Setup**
❖ **Lab #2: Select and Configure an Output Display**
❖ **Lab #3: Play live Video and Recorded Video on the Target Display**

Day 2

➢ i.MX8M Video Processing Unit (VPU)

- Video Processing Unit (VPU)
  - OpenMAX IL API
  - Hantro HW decoder and post processor (G1 & G2)
  - OpenMAX IL API functionality
  - Decoder features
  - Input & output buffers
  - Video frame storage formats
  - Interface functions

➢ i.MX8M Audio

- Sony/Philips Digital Interface (SPDIF)
  - Overview
  - Transceiver data interface block diagram
  - SPDIF receiver functional description
  - SPDIF transmitter functional description
  - Which SPIDF exceptions can trigger an interrupt?
- Synchronous Audio Interface (SAI)
  - Block diagram
  - Main features
  - Modes of operation
  - Reset and clocks
  - Synchronous modes
  - Frame sync configuration
  - Data FIFO
  - Interrupts and DMA requests
- Codecs supported

❖ **Lab #4: Decode 4K (H264/VP9) Video File and Stream to HDMI**
❖ **Lab #5: Capture Video from Camera (MIPI-CSI)**
❖ **Lab #6: Apply Face Detection on Captured Frames and Send to the Display**

Day 3

➢ i.MX8M Graphic Processing Unit (GPU)

- GPU fundamentals
  - What is a GPU?
  - Real time rendering and its importance
  - GPU types for i.MX8
  - GC7000 Lite architecture
  - Graphics pipeline front end
  - Unified shader engine: Vertex
  - 3D rendering engine
  - Unified shader engine: Fragment
  - Texture engine
  - Pixel engine
  - Vulkan support
  - i.MX8M display pipeline
  - i.MX8M DPR display controller cache
  - GPU performance
  - Supported APIs
  - GPU debug tool
  - Graphics decompression
  - Decompression and tile to raster conversion
  - Display, prefetch and resolve
  - Scaler
  - Look up table load
  - HDR10 image processing
  - Color sub-sampler
  - Write scale and read surface

➢ i.MX8M HDMI Display Transmitter Controller (HDMI TX)

- Overview
- Block diagram
- Main features
- Management and control interface
- Audio interface
- PHY interface
- On chip memories
- Video packing
- Audio packing
- Info-frame packing
- HDCP

- Clocks and reset

- **Lab #7: Filter Implementation (Edge Detection) on a Live Video Stream on Top of CPU**
- **Lab #8: Filter Implementation (Edge Detection) on a Live Video Stream on Top of GPU**
- **Lab #9: Measure and Compare Performance Between CPU and GPU**