

VHDL-2008 for Synthesis with Quartus Prime Pro

Course Description

This course introduces the new and changed features of VHDL-2008, in order to improve and enhance hardware engineer's skills.

The course goes into great depth and teaches the advanced features of the VHDL-2008 language through code examples, shows how they improve the language as a tool for design and verification, and guides how to employ them in new designs.

The training covers the synthesized new structures, operators, and highlight the hardware result, using the Quartus Prime Pro.

The course combines 50% theory with 50% practical work in every meeting. The practical labs cover all the theory.

This course also enriches digital engineers with many years of experience.

Course Duration

2 days (plus final exercise as homework)

Goals

1. Become familiar with the expand and new IEEE Packages
2. Apply advanced arithmetic/logic operations on arrays and scalars
3. Be familiar with VHDL-2008 new operators
4. Write generic models using the new relaxed rules for synthesis
5. Use generic functions and procedures for synthesis include operator and function overloading
6. Use revised rules for port map, aggregates, port modes
7. Use powerful new generate statements
8. Define generic types, constants
9. Use package in a process and subprogram
10. Write advanced test-benches using external names, force & release, and revised text I/O

Intended Users

Hardware engineers who develop FPGAs and would like to enhance their skills, in order to become experts with VHDL-2008 new language features for design and verification

Previous Knowledge

FPGA design, VHDL

Course Material

1. Simulator: Modelsim
2. Synthesizer and Place & Route: Quartus Prime Pro

Table of Contents

Day #1

- **Introduction to VHDL-2008**
 - Why VHDL-2008?
 - Expanded and new IEEE libraries
- **VHDL-2008 New Features Overview**
 - Expanded declarative part on an Entity/Architecture
 - Multi-line comment
 - Simplified sensitivity list
 - The ?? condition operator
 - Simplified condition
 - +/- overload for scalar values
 - Unary reduction operators
 - Matching relational operators
 - Matching operators for arrays
 - Minimum & maximum functions
 - Mod & rem for physical types
 - Shift operations overloading
 - Conditional & selected assignments in process
 - Use unaffected keyword



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- Case? And with select? Statements
- Locally static expressions
- Enhanced bit string literals
- Referencing generics in generic lists
- Context declarations & rules
- Unconstrained array types enhancement
- Unconstrained record
- Type conversions
- 'element attribute
- 'subtype attribute
- New array types
- Fixed & float data types
- Ports revision (entity and procedure)
- Slices in aggregates
- Select logic in port map
- Powerful generate statements
- Recursive generate statements

❖ **Hands-on labs**

Day #2

- **VHDL-2008 Modularity**
 - Enhanced generics
 - Generic types
 - Generic lists in packages
 - Local packages
 - Generic lists in subprograms
 - Generic subprograms
 - Generic packages
 - Enhanced Packages
 - Package in package
 - Package in subprogram
 - Generic lists in subprograms
 - Generic subprogram & rules



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- **VHDL-2008 Verification**

- Testbench enhancement with External names
- External constant name in an expression
- External names & FSM
- Force and release signal assignments and rules
- Conditional force statement
- Integrated PSL
- IP encryption
- VHDL procedural interface (VHPI)
- OS-VVM
- Improved I/O
 - TO_string functions
 - Justify function
 - Newline formatting
 - Read & Write operations
 - The TEE procedure
 - The Flush procedure

- ❖ **Hands-on labs**

- **Final Exercise: Design & Implement a Small Project with VHDL-2008**

- Project introduction & Theory
- Project design stage
 - Using VHDL 2008 enhancements
 - Using functions & procedures
 - Design for reusability
- Project verification stage
 - Writing test vectors
 - Reading and writing files with text I/O and std_logic_textio packages



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