



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

altera™ solution acceleration partner

Achieving Timing Closure in Altera FPGAs

Course Description

This course provides all necessary theoretical and practical know-how to analyze and fix timing failures for variety use cases in Altera FPGAs.

The course goes into great depth and touches upon every aspect of timing failures due to setup and hold negative slack, I/O input/output delays, reset issues, CDC, high fanout, global clock networks, over constrained design, as well as timing exceptions.

The course begins with methodology for timing closure, the FPGA architecture, and the effect of incorrect timing constraints, and HDL coding considerations.

The course continues by reviewing the various analysis tools in the Quartus Prime Pro software, such as Design Assistant, Fitter reports, Snapshot Viewer, Chip Planner and Design Metrics reports.

The course continues with an in-depth solution for various timing failures use cases such as CDC congestion, too many logic levels, high fanout, conflicting SDC assignments, conflicting location assignments, tight timing requirements, clock crossing, and clock skew.

The course includes extensive practical work. The practical labs cover all the theory.

Each attendee receives an official certificate from Altera (Exam must be passed)

Course Duration

2 days



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Goals

1. Understand TimeQuest reports and when to use each
2. Writing correct SDC constraints
3. Apply timing exceptions in SDC
4. Become familiar with the recommended timing closure methodology
5. Analyze and fix various timing problems
6. Use efficiently the chip planner, TimeQuest, RTL and Technology view for advanced timing analysis

Intended Users

Hardware engineers who develop FPGAs and would like to enhance their skills, in order to fix and solve simple and complex timing issues in their projects, and acquire better expertise with TimeQuest and other Quartus Prime tools for timing issues analysis.

Prerequisites

FPGA design, VHDL/Verilog, TimeQuest basic knowledge, Quartus Prime Standard/Pro

Course Material

1. Quartus Prime Pro
2. Course book
3. Lab's handbook and lab files



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Table of Contents

Day #1

❖ **Timing Closure Methodology**

- The imperfect world
- Setting expectations
- Goal of timing optimization methodology
- Timing closure challenges
- Methodology for timing closure

❖ **Altera FPGA Architecture Review**

- DSP block
- M20K RAM
- Hyperflex architecture

❖ **Timing Constraint**

- Timing constraints requirements
- Verifying timing constraints
- Effect of incorrect timing constraints

❖ **HDL Coding Considerations**

- HDL coding effect
- Analyze arithmetic circuit paths
- Use the assignment editor for DSP block balancing
- If/Else & Case statements issues
- If/Else & Case statements recommendations

❖ **Too Many Logic Levels Issue**

- Too many logic levels effect



- Logic levels in technology map viewer
- Solutions for too many logic levels

❖ Designing for Hyper-Retiming

- What prevents retiming?
- Path endpoint restrictions
- Common design situations preventing retiming

❖ Designing Resets

- Reset usage limitation concept
- Reset synchronizer
- Reset IP
- X-propagation

❖ Clock Domain Crossing

- Synchronization circuits
- Clock domain crossing: QSF
- Clock domain crossing: SDC

Day #2

❖ Design Assistant

- Design Assistant introduction
- Design areas checked
- Timing closure specific checks
- Design Assistant reports
- Examples of timing issues analysis
- Cross-probe from Design Assistant reports to chip Planner



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❖ **Fitter Reports**

- Notable Fitter reports
- Control signals
- Duplication summary
- Physical RAM information
- Routing usage summary
- Estimated delay added for Hold timing
- Retiming limit details
- Fast Forward Timing Closure Recommendations

❖ **Snapshot Viewer**

- Snapshot viewer introduction
- Tasks and commands
- Enable intermediate Fitter snapshots
- Accessing Snapshot viewer

❖ **Chip Planner**

- Main window
- Tasks
- Reports
- Cross-probe from Quartus software
- Reports with cross-probed modules
- Deactivate reports

❖ **Design Metrics Reports**

- Report logic depth
- Report neighbor paths
- Report register spread
- Report route net of interest



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- Report retiming restrictions
- Report pipelining information
- Report detailed pipelining
- Report bottlenecks

❖ **Fixing Timing Issues**

- Analyze CDC issues
 - Solutions for CDC issues techniques
 - Analyze too many logic level issues
 - Solutions for too many logic levels techniques
 - Analyze high-fanout issues
 - Solutions for high-fanout techniques
 - Analyze placement issues
 - Solutions for placement issues
 - Analyze tight timing issues
 - Solutions for tight timing issues
 - Use the advanced settings for synthesis and fitter
 - Use the seed sweep technique
 - Use the Design Space Explorer II (DSE II)
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- **Lab #1: Analyze and Fix Timing Failures**
 - **Lab #2: Analyze and Fix Complex Timing Failures**
 - **Lab #3: Timing Optimization using a PLL**



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