Designing with STM32MP157 SoC

STM32MP157 microprocessors are based on a flexible architecture consist of a Dual Arm® Cortex®-A7 core running at 650 MHz and Cortex®-M4 at 209 MHz combined with a dedicated 3D graphics processing unit (GPU), MIPI-DSI display interface and a CAN FD interface. Specifically designed to accelerate 3D graphics in applications such as graphical user interfaces (GUI), menu displays or animations, the STM32MP157 3D OpenGL ES 2.0 graphics engine works together with an optimized software stack design for industry-standard APIs with support for Android™ and Linux® embedded development platforms.

Course Description

STM32MP157 is a feature rich SoC, encapsulating many sub-modules, which makes it a challenge to comprehend. ***'Designing with STM32MP157 SoC'*** is a 3-day training that aims providing a deep understanding of the STM32MP157 SoC and speed up the software design process, enabling you to focus on your added value as soon as possible.
Practical work enriches the learning experience and provides an added value to our students, therefore this training blends both, technical data deep-dive and practical labs on hardware platform. During the labs, you'll take an active part in coding and building functional use-cases, both on Cortex®-M4 and Cortex®-A7. You'll experience developing applications and kernel modules under Linux, learn about frameworks like Gstreamer, and write bare-metal/ free-RTOS software for the Cortex®-M4.

Course Goals

- Introduce STM32MP157 architecture
- Introduce heterogenous ARM cores: Cortex®-A7 and Cortex®-M4
- Introduce STM32MP157 multimedia, graphics and audio capabilities
- Introduce the clock management, reset, power management
- Introduce the STM32MP157 memory architecture and capabilities
- Introduce the STM32MP157 Boot process
- Introduce the developments tools, used to develop software on both micro-processors

Target Audience

Software engineers that would like developing software and BSP for platforms based on STM32MP157 SoC.

Course Duration

3 days

Target platform

STM32MP157C-DK2 Discovery Board, by ST, is used as the development platform for the lab.

Prerequisites

- Computer architecture background
- Experience in developing embedded systems
- C/C++ knowledge
- Familiarity with ARM architecture is an advantage
- Familiarity with Linux is an advantage

Day 1

➢ Introduction to the STM32MP157 Family

- ❖ STM32MP157 processor values
- ❖ STM32MP157 processor portfolio
- ❖ STM32MP157 main target applications
- ❖ STM32MP157 key features
- ❖ STM32MP157 flavors, block diagrams and differences
- ❖ STM32MP157 qualification levels and package type
- ❖ i.MX8M Mini evaluation boards, SoM, and Software support

Lab #1: Board and Tools Bring-up

➢ CPU Platform

- ❖ Cortex-A7 CPU platform overview
  - Cortex-A7 block diagram and features
  - Performance monitor unit
  - VFPv4 (floating point coprocessor)
  - Neon coprocessor
  - Virtualization and LPAE support
  - Timers
  - Debug features
  - Caches and branch prediction
  - MMU
  - Cache coherency
  - Generic Interrupt Controller
  - TrustZone

Lab #2: Measuring Application Performance and memory implications using linked lists

- ❖ Cortex-M4 platform overview
  - Cortex-M4 features
  - M-profile instructions
  - Core register set
  - Processor pipeline
  - Cycle counting
  - Memory map
  - Bitwise memory access
  - Bit banding

- Modes privilege and stacks
- Interrupts and exceptions
- Memory Protection Unit (MPU)
- Tightly Coupled Memory (TCM)
- Cache features
- Processor core, space and Backdoor port accesses
- SRAM accesses
- Power management
- Core debug
- System timer
- Floating point unit
- Cortex-M4 use case

Lab #3: Configure the MPU with Different Access Permissions and Identify Stack Overflow

Day 2

➢ STM32MP157 Memory System Overview

- ❖ Internal memory (Cache, SRAM, ROM)
- ❖ Nand/Nor flash storage
- ❖ SD/eMMC storage

➢ STM32MP157 Memory interfaces

- ❖ SPI
- ❖ Quad SPI
- ❖ Flexible memory controller
- ❖ SDMMC

➢ STM32MP157 DRAM controller (DDRCTRL)

- ❖ DDRCTRL main features
- ❖ DDRCTRL block diagram
- ❖ DDRCTRL architecture overview
- ❖ DDRCTRL functional description

- **STM32MP157 peripherals**
  - Timers
  - UART
  - I2C

- **STM32MP157 Inter-Processor communication controller (IPCC)**
  - IPCC main features
  - IPCC block diagram
  - IPCC simplex channel mode
  - IPCC half duplex channel mode
  - IPCC interrupts
  - Remote Processor Msg (RPMSG)
  - OpenAMP

Lab #4: Open a communication channel and transfer messages between the Cortex-A7 and Cortex-M4

- **STM32MP157 Connectivity**
  - CAN
  - USB
  - Ethernet

- **STM32MP157 Reset and clock control (RCC)**
  - RCC main features
  - RCC block diagram
  - RCC functional description – reset part
  - RCC functional description – reset part
  - RCC interrupts
  - RCC application information

- **STM32MP157 Power Control (PWR)**
  - PWR main features
  - PWR block diagram
  - PWR power supplies
  - PWR power supply supervision
  - PWR power management
  - PWR low power modes
  - PWR interrupts
  - PWR TrustZone security

Lab #5: Low power mode wakeup

➢ STM32MP157 DMA

- ❖ DMA main features
- ❖ DMA block diagram
- ❖ DMA transactions
- ❖ DMA streams & Arbiter
- ❖ Source, destination and transfer modes
- ❖ DMA interrupts
- ❖ DMAMUX implementation
- ❖ MDMA functional description
- ❖ Linux DMA Engine driver

Lab #6: Measuring the "memcpy" function using DMA, Cortex-A7, and Cortex-M4

STM32MP157 Boot

- Standard Linux boot chain
- STMP32MP1 boot chain
- Boot mode selection
- Boot devices supported
- Trusted boot chain

Day 3

STM32MP157 Graphics Overview

- Multimedia components
  - LCD-TFT display controller (LTDC)
  - GPU
  - DSI Host
  - Digital camera interface (DCMI)
  - SPDIF receiver interface (SPDIFRX)
  - Serial Audio Interface (SAI)
- LCD-TFT display controller (LTDC)
  - LTDC main features
  - LTDC block diagram
  - LTDC global configuration parameters
  - Layer programmable parameters
  - LDTC interrupts
- GPU
  - What is a GPU?
  - Graphics pipeline overview
  - Fixed & programmable pipelines
  - GPU main features
  - GPU general description
  - Supported APIs
  - GPU performance

- Digital camera Interface (DCMI)
  - DCMI main features
  - DCMI block diagram
  - Capture modes
  - Crop feature
  - JPEG format
  - Data format description
  - DCMI interrupts

Lab #7: Stream a video file over the network