



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

altera™ solution acceleration partner

Partial Reconfiguration with Altera FPGAs

Course Description

This course provides all necessary theoretical and practical know-how to use the partial reconfiguration methodology and design flow in Altera FPGAs, in order to reprogram one or more parts of a design dynamically, while the rest of the design continues to operate.

The course begins with an overview of what is partial reconfiguration, its main applications, PR definitions for region, partition, persona, PR host and control block.

The course continues with PR hierarchical design flow, design partition recommendations, tools and LogicLock regions.

Then timing closure is discussed for PR, changing port values during PR, management of global resources, debugging PR regions.

The course teaches how to design PR host (internal or external), PR host IP for region management, PR controller IP, how to program and configure PR, and PR project full design flow in greater details.

The course includes extensive hands-on labs.

Each attendee receives an official certificate from Altera and from Arm (Exam must be passed).

Course Duration

2 days



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Goals

1. Understand what partial reconfiguration (PR) is and its many uses
2. Learn how to go through the PR design flow
3. Prepare a design for PR
4. Integrate a PR host
5. Compile the PR design to create the required bitstream files

Intended Users

Hardware engineers who develop with Altera FPGAs (Arria 10/Stratix10/Agilex) and would like to apply the PR methodology into their design.

Prerequisites

1. FPGA design experience
2. VHDL/SystemVerilog
3. Quartus Prime Pro
4. TimeQuest
5. Avalon bus
6. ModelSim/Questa

Course Material

1. Quartus Prime Pro
2. Course book
3. Lab's handbook and lab files
4. Altera Stratix 10 GX FPGA Development Kit (optional)



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Table of Contents

Day #1

❖ PR Overview

- What is Partial Reconfiguration (PR)?
- PR applications
- Benefits of PR
- PCIe interface attached accelerators
- Example application
- PR glossary
- PR considerations
- PR host
- PR control block (Arria 10 only)
- PR regions
- Supported reconfiguration types for resources
- Combined reconfiguration modes
- PR hierarchical design flow
- Other PR flows (HPR, SUPR)
- Static Update PR

❖ PR Design Partitions & Logic Lock Regions

- What are design partitions?
- Design partition uses
- Design partitions and revisions for PR
- General design partition recommendations
 - Register both partition input & output ports
 - Minimize cross-boundary paths
- Design partitions tools
 - Setting design entities as PR partitions
 - Design partitions window
 - PR partition .qsf assignments
- Logic Lock regions
 - What is a Logic Lock region?
 - Logic Lock floorplanning for PR
 - Defining Logic Lock regions
 - Logic Lock region options/assignments
 - Routing regions
 - Logic Lock regions window
 - Ways to create regions



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- Creating regions from logic
- Region properties
- Logic Lock region .qsf assignments
- Floorplanning recommendations, tips & strategies
- Stratix 10 bitstream optimization

❖ **General Design Guidelines & Restrictions**

- Starting timing closure for PR
- Persona interfaces
- Upper-level port “superset”
- PR region diagram
- Examples
 - Example: persona port lists
 - Example: port list superset
 - Example: upper-level instantiation
 - Example: port map for each persona file
- Persona initial conditions
- Changing port values during PR
- Freezing PR region ports
- Static region freeze logic examples
- Global signal usage
- Manual assignment of global resources
- Other global resource use considerations
- PR region global signal type use limitations
- PR region reset recommendations
- Example of synchronous reset subdomains
- Prevent errant writes to initialized memories
- Prevent errant writes with clock gating
- On-chip debugging tool support
- Static region debug tool placement
- Signal Tap logic analyzer in static region
- PR region debugging
- Signal Tap logic analyzer in PR region

- **Lab#1: Preparing a Design for PR**

❖ **Other Reconfiguration Solutions**

- FPGA reconfiguration types
- What is transceiver reconfiguration?
- Example uses
- Transceiver reconfiguration steps
- Transceiver reconfiguration with PR strategy



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- PLL reconfiguration
- Example uses
- PLL reconfiguration controller
- PLL reconfiguration diagram
- PLL reconfiguration with PR strategy

Day #2

❖ PR Host Design & Implementation

- PR host
- Configuration RAM (CRAM)
- Configuration frames (Arria 10 devices)
- PR bitstreams
- PR CB interface (Arria 10 devices)
- Control block interface main signal functions
- Putting it all together
- Sequence of operations for PR host
- PR control and handshaking timing

❖ PR Host IP for Region Management

- PR IP
- PR region controller IP
- Region controller parameters
- Complete region controller timing diagram
- Avalon-MM or Avalon-ST freeze bridge IP
- Memory-mapped freeze bridge IP behavior
- Streaming freeze bridge IP behavior
- Freeze bridge IP parameters

❖ PR Controller IP

- PR controller IP overview
- Stratix 10 PR controller IP block diagram
- Arria 10 PR controller IP block diagram
- Required CRC block (Arria 10 only)
- Control block interface controller
- PR bitstream compression
- PR bitstream encryption
- Data source controller
- JTAG debug interface



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- Startix 10 PR controller IP parameters
- Arria 10 controller IP parameters
- Main PR IP ports
- Additional ports (Arria 10 only)
- PR controller IP timing diagram
- Avalon Memory-Mapped interface
- Instantiate PR blocks (Arria 10 only)
- PR controller IP as part of internal host
- Manual block instantiation in Arria 10 devices

- **Lab#2: Integrating a PR Host**

❖ External Host Implementation

- PR with external host
- Enabling external PR host pins
- Enable PR pins for external host
- PR external host pin considerations
- Arria 10 PR controller IP external host use
- PR external controller for Startix 10 FPGA IP
- Setting configuration scheme
- Startix 10 external host setup

❖ Programming & Configuration for PR

- Why configuration?
- FPGA configuration RAM
- FPGA programming
- Arria 10 FPGA supported configuration scheme
- Stratix 10 FPGA supported configuration scheme

❖ PR Design Flow

- Recall: PR design flow
- PR project flow
 - Create project base revision
 - Define PR partitions & Logic Lock regions
 - Cross probe to chip planner
 - Implement host, internal or external, custom logic or IP
 - Fully compile and verify base revision
 - Steps required for complete PR simulation
 - Export base revision's static region (including SUPR flow)
 - Create implementation revisions
 - Compile implementation revisions



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- Timing closure for PR
- Aggregate revisions for multiple PR region timing
- **Lab #3: Creating & Compiling Implementation Revisions**

❖ **Generated Files**

- Full chip configuration
- PR-related configuration files
- Assembler generation of programming files
- Programming file conversion
- Convert .pmsf to .rbf
- Output file options
- Input file options
- .pmsf file properties (Arria 10 only)
- Convert .pmsf to .rbf from command line
- .pmsf file merging
- PR over JTAG
- PR in the programmer
- SUPR region programming file use & updating
- Using flash memory to store PR data
- Convert .rbf to .flash
- Write to flash with Nios flash programmer
- **Lab #4: Testing the PR Design**



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