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20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

# altera™ solution acceleration partner

## Introduction to Nios V Processors

### Course Description

This course provides all theoretical and practical know-how to create and manage software projects for Nios V processors.

The course starts by reviewing the Nios V processor variants as well as the architectures difference.

Then, you learn how to integrate Nios V to Quartus project using the hardware design flow in the Platform Designer tool and generate the files for software developer.

The course continuous by going through the software development flow including BSP editor, HAL, linker script, timers, interrupt and exception handling, etc.

The Ashling RiscFree IDE for Altera FPGAs is also covered and used in the hands-on labs.

The course ends by discuss the various booting and configuration options and how to debug Nios V processors.

The course includes extensive hands-on labs to experience with the theory via practical work.

**Each attendee receives an official certificate from Altera** (Exam must be passed)

### Course Duration

2 days



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## Goals

1. Become familiar with Altera Nios V processor, its capabilities and when to use it
2. Design Nios V system with the Platform Designer tool
3. Develop BSP & application software for Nios V processor
4. Accessing peripheral through Hardware Abstraction Layer (HAL)
5. Develop BSP for Nios II processor
6. Debug simple and complex Nios II systems, including multi-processor systems
7. Use custom instructions with the Nios V design
8. Configure peripherals and timers

## Intended Users

Hardware and software engineers who would like to integrate Nios V into their project.

## Prerequisites

- Embedded system software design
- C/C++ programming

## Course Material

1. Course book
2. Lab handbook with lab files
3. Stratix 10 GX FPGA development kit
4. Quartus Prime Software Pro Edition v25.3 with Ashling RiscFree IDE for Altera FPGAs, license for Nios V/g and Nios V/m processors.
5. Stratix 10 Development Kit device support installed



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## Table of Contents

### Day #1

#### ❖ Introduction to Nios V Processors Architecture

- What is Nios V processor?
- Advantages of Nios V processors
- RISC-V
- Nios V resources
- Nios V architecture versions (V/m, V/g, V/c)
- Nios V architecture in details
- Nios V/g Lockstep implementation
- Nios V/g branch prediction
- Nios V/g custom instructions

#### ❖ FPGA Hardware Design Flow

- Integrating the design to a Quartus project
- Creating a Nios V processor design
- Saving and adding the custom instruction with Nios V/g
- Implementing custom instructions
- Component editor
- Using the command shell
- Debugging the Nios V/c processor

### Day #2

#### ❖ Software Build Tools and System Design with Nios V Processors

- Nios V processors software development flow
- Nios V BSP Editor and generation
- Linker script
- Linking behavior



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- System clock timer
- Timestamp timer
- Character mode devices
- System description file
- Custom instructions
- Hardware Abstraction Layer (HAL)
- Nios V embedded project structure
- Supported drivers in HAL
- Enhanced HAL interrupt API
- Traps
- Exception & interrupt handling
- CLIC & CLINT
- Shadow register

#### ❖ **Parameter Configuration for Nios V Processors & Software Development**

- Application files
- Application project
- Project navigation inside Ashling RiscFree IDE for Altera FPGAs
- Ashling Visual Studio Code extension
- BSP generator in Ashling VSC
- Nios V App Project Generator in Ashling VSC
- Nios V processors software development flow
- Altera FPGA embedded development tools
- File tree directory

#### ❖ **Booting & Configuration Options**

- Nios V processors booting solutions
- Booting flow: execute in place
- Booting flow: program copied to RAM
- Detailed boot flow
- System startup in HAL
- System initialization
- Flash memory devices



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- Memory system
  - Boot memory
  - QSPI execute in place
  - QSPI GSFI bootloader
  - QSPI SDM bootloader
  - OCRAM execute in place
  - TCM execute in place
  - Platform Designer and booting configuration
  - Debugging Nios V software project with Ashling RiscFree
  - Implementing TinyML with Nios V processors
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- **Lab #1: Hardware Design Tools for Nios V Processor**
  - **Lab #2: Using the Development Kit with Nios V/m Processor**
  - **Lab #3: Peripherals and Timer Configuration**
  - **Lab #4: Using Nios V/g Custom Instructions**



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