HandsOn Training

Intel® FPGA Technical Training

Synchronization Circuits Design in Intel FPGAs

Course Description

This course focuses on synchronization circuits design in Intel FPGAs using TimeQuest to measure MTBF.

The course starts with the motivation to increase circuit reliability by understanding synchronization circuit role for cross clock domain design.

The course continues with deep dive study of the synchronization techniques for various use cases, then choosing the right solution for your specific design.

The course covers also the synchronization circuit design for reset.

The course ends with the flow in Quartus Prime to make sure the software identifies your synchronization circuits, then analyze their reliability (using circuits for cross clock domain designs MTBF calculations) in TimeQuest.

The course embeds hands-on lab that encapsulate all theory into one final practical work, where the participant will design a handshake synchronization protocol.

Course Duration

1 day

Goals

1. Increase circuit reliability and performance by applying synchronous design techniques
2. Be familiar with metastability formula
3. Understand the synchronization circuits role in synchronous design
4. Choose the right synchronization solution for your design
5. State advantages and disadvantages of synchronous and asynchronous reset
6. Apply a synchronization circuit for an asynchronous reset
7. Design synchronization circuits for multiple clock domain designs

Intended Users

FPGA engineers who would like to enhance their skills and design reliable multi-clock domains FPGA projects, and analyze their solution in TimeQuest.

Previous Knowledge

Intel FPGAs architecture

Quartus Prime software

ModelSim

Course Material

1. Simulator: Modelsim
2. Synthesizer and Place & Route: Quartus Prime
3. Course book (including labs)

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  - Unique characteristics of MTBF

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- **Hands-On Lab: Build Handshake Synchronization Protocol**