Intel® FPGA Technical Training

Quartus Prime Foundation

Course Description

This course provides all theoretical and practical know-how to design programmable devices of Intel with Quartus Prime design software.

The course combines 50% theory with 50% practical work in every meeting. The practical labs cover all the theory.

The course starts with an overview of the Quartus Prime design software features, Quartus Prime projects types and management, design methodology, and using IP cores from the IP catalog. Qsys system integration tool, state machine editor, memory editor, Altera SD for OpenCL, and DSP Builder are also introduced in high level.

The course continues with Quartus Prime compilation flow, incremental compilation concept, working with messages, viewing compilation reports, RTL and technology views, state machine viewer, and how to use the chip planner tool.

The course also touches upon synthesis and Place & Route settings and assignment editor, optimizations, design assistant and various advisors.

The course ends with I/O planning with the pin planner, with the BluePrint Platform Designer, and programming and configuration of FPGA/CPLD.

Course Duration

2 days

Goals

1. Create a new Quartus Prime project
2. Choose supported design entry methods
3. Compile a design into a programmable logic device
4. Locate resulting compilation information
5. Create design constraints (assignments & settings)
6. Manage I/O assignments
7. Prepare for programming/configuring a programmable logic device

Intended Users

Hardware engineers who program with VHDL/Verilog languages and would like to be specialized with Intel FPGAs and Quartus Prime software

Previous Knowledge

VHDL/Verilog beginners and advanced users who are new to Intel FPGAs.

Course Material

1. Synthesizer and Place & Route: Quartus Prime
2. Course book (including labs)

Table of Contents

Day #1

- **Introduction to Programmable Logic Devices**
  - CPLD architecture and design consideration
  - FPGA architecture (LUT, FF, PLL, DSP Block, Embedded RAM, Embedded Processor, Programming)

- **Introduction to Intel FPGAs**
  - CPLD : MAX V, MAX II
  - FPGA : Max 10 Cyclone, ARIA, STRATIX, SoC ARM based
  - FPGA: Gen 10 devices and SoC

- **Introduction to Quartus Prime Software**
  - Lite Edition, Standard Edition and Pro Edition
  - Quartus Prime design software features
  - Quartus Prime default operating environment
  - Tips and tricks advisor
  - Built in help system
  - Custom task flow
  - TCL and command line help

- **Quartus Prime Projects**
  - Project creation and project types
  - Intel design store
  - EDA tool settings
  - Quartus Prime project files and folders
  - Constraint files & assignment priority
  - Project management (archive, restore, copy, revisions, clean)
  - IP management tools

❖ **Lab #1: Create a Project in Quartus Prime**

- **Design Methodology**
  - Typical PLD design flow
  - Design entry methods (schematic, HDL, EDIF)
  - Altera IP cores
  - IP catalog
  - System design entry with Qsys
  - State machine editor
  - Memory editor
  - DSP Builder standard/advanced blocksets
  - Open Computing Language (OpenCL)
  - Synthesis and P&R
  - Programmer

❖ **Lab #2: Use IPs from the IP Catalog and the Memory Editor**

- **RTL Coding Guidelines for Quartus Prime Integrated Synthesis**
  - Synthesis directives and attributes
  - Fixed output registers
  - RAM inference
  - Latch inference
  - Combinational loops
  - Finite state machine coding styles

- **Lab #3: Use Synthesis Attributes to Affect Quartus Prime Synthesis Results**

Day #2

- **Quartus Prime Compilation**
  - Quartus Prime full compilation flow
  - Processing options
  - Notification center
  - Compilation design flows
  - Incremental compilation concept
  - Reducing compile times
  - Message windows
  - Viewing compilation results
  - Dynamic synthesis report
  - Netlist viewers
  - State machine viewer
  - Chip planner
  - Resource property editor

❖ **Lab #4: Compile a Project in Quartus Prime and Locate Information in the Compilation Report**

- **Settings & Assignments**
  - Synthesis and fitting control
  - Device settings
  - Version compatible database
  - Consolidated compiler optimization settings (synthesis & fitter)
  - Assignment editor features
  - Assignment groups
  - Updating .qsf file
  - Assignment Tcl command
  - Export assignment
  - Design assistant
  - Advisors

❖ **Lab #5: Create a New Revision and Make Design Constraints using the Assignment Editor**

- **I/O Planning**
  - I/O planning need
  - Creating I/O related assignments
  - Pin planner tool
  - Assigning pin locations using pin planner
  - Pin planner tasks & report windows
  - Pin migration view
  - Reserved and unused I/O pins
  - Back annotation
  - Verifying I/O assignments
  - I/O rules checked
  - I/O assignment analysis output
  - Validating I/O pin-put
  - I/O planning with the BluePrint Platform Designer tool
  - Import/export via CSV
  - .qsf editing and scripting
  - Global pin settings
  - Using synthesis attributes in HDL

❖ **Lab #6: Assign I/O Pins and Perform I/O Assignment Analysis, Back Annotate Pin Assignments, and Use Pin Migration View**

- **Programming & Configuration**
  - Programming files (sof, pof, jam/jbc, jic)
  - Programming file conversion
  - Quartus Prime programmer