Designing with STM32F10 Family

Course Description

Designing with STM32F10 Family is a 3 days ST official course.

The course provides all necessary theoretical and practical know-how for start developing platforms based on STM32F10x.

The course begins with an introduction to STM32F microcontroller families and focuses on Cortex-M3 architecture.

The course continues with an in-depth study of the memory organization, reset unit, interrupts handling, low power modes, and all the SoC peripherals such as I/O ports, ADC, RTC, USART, I2C, DAC, SPI, CAN, USB, SDIO, FSMC, Timers, FIO, DMA and CRC.

The course also employs hardware and software design tools, and combines 50% theory with 50% practical work in every meeting.

Course Duration

3 days

Goals

1. Become familiar with STM32F families
2. Become familiar with ARM Cortex-M3 architecture
3. Become familiar with STM32F10x peripherals
4. Become familiar with hardware and software design tools
5. Build a new project using the development tools
6. Work with Firmware libraries

Target Audience

Software and hardware engineers who would like start developing with STM32F10x microcontroller

Prerequisites

- Computer architecture background
- Experience in C programming
- Experience in developing embedded systems

Course Material

- STMCube
- ST Eval board
- Course book (including labs)

Agenda

Day #1

- **Cortex-M3 Architecture**
  - Cortex-M3 architecture overview
  - Performance
  - Comparison to ARM7
  - Bit banding
  - Integrated debug capabilities
  - Privilege, modes and stacks
  - Register set
  - Interrupt and real time capabilities
  - Power management
  - Code size and performance gain using Cortex-M3
  - AR7 to Cortex-M3 migration

- **STM32 Tools Overview**
  - Hardware support tools
  - Software support tools
  - Firmware libraries

- **STM32F1 In Details**
  - Introduction to STM32F10x family
  - STM32F10x block diagram
  - Memory mapping and boot modes
  - System architecture

- **Embedded FLASH**
  - Flash features
  - Flash operations
  - Flash memory accelerator
  - Information block
  - Flash protection
- **Lab #1:** Tool-chains and board install

Day #2

- **Cyclic Redundancy Check (CRC)**
  - CRC features
- **Direct Memory Access (DMA)**
  - DMA features
  - DMA request mapping
  - DMA latency
  - DMA and Bus occupation
- **Lab #2:** DMA memory to memory transfer
- **Power Control (PWR) and Backup Domain (BKP)**
  - Power supply
  - Power on reset (POR)/ Power down reset (PDR)
  - Programmable voltage detector (PVD)
  - Backup domain
  - Low power modes
- **Reset and Clock Control (RCC)**
  - Reset sources
  - On chip oscillators
  - LSI calibration using TIM5_CH4
  - Clock scheme
- **Lab #3:** Clock configuration, clock security system
- **General Purpose & Alternate Function I/O (GPIO & AFIO)**
  - GPIO features
  - GPIO configuration modes
  - AFIO features
- **Lab #4:** GPIO & Bit Band
- **External Interrupt/Event Controller (EXTI)**
  - EXTI features
- **Lab #5:** NVIC example

- **Real-Time Clock (RTC)**
  - RTC features
- **Lab #6:** Low power and EXTI

- **Window Watchdog (WWDG) & Independent Watchdog (IWDG)**
  - WWDG features
  - IWDG features

- **Advanced Control & General Purpose Timers**
  - 8 timers with advanced control features
  - Features overview
  - Counter modes
  - Update event
  - Counter clock selection
  - General purpose timer features
  - Advanced timer features
  - Capture compare array
  - Input capture mode
  - PWM input mode
  - Output compare mode
  - PWM mode
  - TIM1 complementary PWM outputs for motor control
  - One pulse mode
  - Encoder interface
  - Hall sensor interface
  - TIMs synchronization

Day #3

- **Analog-to-Digital Converter (ADC)**
  - ADC features
  - ADC block diagram
  - ADC regular & injected channels group
  - Analog sample time
  - Sequencer
  - ADC conversion modes
  - ADC discontinuous conversion mode
  - ADC data alignment
  - ADC analog watchdogs
  - DMA
  - ADC dual modes
- **Lab #7:** ADC using DMA

- **Digital-to-Analog Converter (DAC)**
  - DAC features
  - DAC channels block diagram
  - DAC output voltage
  - Single DAC channel data format
  - DAC conversion triggers
  - Noise wave generation
  - Triangle wave generation
  - DMA
  - Dual DAC channel mode and data format

- **Serial Peripheral Interface (SPI)**
  - SPI features
  - Data frame format
  - Full duplex communication
  - Simplex communication
  - NSS HW & SW management
  - Multi master : SS output management
  - CEC calculation

- **I2S Mode**
  - I2S features
  - I2S audio protocol
  - Data format and packet frame
  - Simplex communication
  - DMA capability

- **Inter Integrated Circuit (I2C)**
  - I2C features
  - DMA capability
  - Dual addressing mode
  - PEC

- **Universal Synchronous Asynchronous Receiver Transmitter (USART)**
  - USART features
  - DMA capability
  - Synchronous mode
  - IrDA SIR encoder decoder
  - Smart card mode
  - Single wire half duplex mode

- **Flexible Static Memory Controller (FSMC)**
  - FSMC features
  - FSMC block diagram
  - FSMC bank memory mapping
  - NOR/PSRAM address mapping
  - NOR/PSRAM interface signals
  - LCD modules interface signals
  - NOR/PSRAM controller
  - NAND address mapping
  - PCCARD address mapping
  - NAND/PCCARD interface signals
  - NAND/PCCARD controller

- **SDIO Interface**
  - SDIO features
  - SDIO block diagram
  - SDIO adapter
  - SDIO DMA requests
  - SDIO hardware flow control
  - SDIO clock configuration
  - SD/SDIO & MMC cards
  - CE-ATA devices

- **Controller Area Network (bxCAN)**
  - CAN features
  - Filter bank scale and mode configuration

- **Universal Serial Bus Interface (USB Device)**
  - USB features
  - Double buffering transfer mode
  - STM32F10x USB developer kit