HandsOn Training

Intel® FPGA Technical Training

Building Interfaces with Arria 10 High-Speed Transceivers

Course Description

In this course, you will learn how you can build high-speed, gigabit interfaces using the 20-nm embedded transceivers found in Arria 10.

You will be introduced to the transceiver architecture and how the transceivers are configured to support various high-speed protocols.

You will learn how to optimize and debug both the digital and analog sections of your transceiver design.

You will gain an understanding of the transceiver reconfiguration controller and how you can use it to fine tune transceiver settings and add flexibility to your transceiver design.

Lastly, you will be made aware of common “gotchas” that occur in transceiver designs and what steps you can take to avoid them.

The course contains hands-on labs to experience with Arria 10 transceiver IP cores configuration, simulation, using the transceiver Toolkit (optional), and enabling Arria 10 transceiver reconfiguration in the Native PHY IP core.

Course Duration

2 days

Goals

1. Implement high-speed serial protocols in Altera 20-nm embedded transceivers
2. Optimize analog settings to improve behavior using Altera tools
3. Employ transceiver reconfiguration to dynamically change transceiver behavior in-system
4. Improve transceiver usage and avoid transceiver design issues by applying an understanding of device architecture to design situations

Intended Users

Hardware engineers who develop with Arria 10 and would like to build gigabit interfaces

Previous Knowledge

FPGA design

Quartus and TimeQuest

Modelsim

SignalTap II

Note: familiarity with high-speed interfaces and transmission protocols is helpful, nut not required

Course Material

1. Synthesizer and Place & Route: Quartus Prime
2. Course book (including labs)
3. Stratix V or Arria 10 Evaluation board (optional)

Table of Contents

Day #1

❖ Transceiver Design Creation

- Introduction to Altera's Transceivers
  - What is a transceiver?
  - Definition: MAC, PCS, PMA
  - Arria 10 FPGAs & SoC transceivers families

- Transceiver Design Creation
  - Arria 10 transceiver documentation
  - Transceiver design creation
  - Transceiver locations
  - Transceiver layout
  - Non-bonded versus bonded
  - Aria 10 GX versus GT channels
  - Aria 10 GT device: 72 transceiver device example

- RX Datapath
  - Receiver path definition
  - Receiver PMA blocks
  - RX PMA functional block descriptions
  - RX polarity inversion
  - Receiver simplified block diagram
  - RX PCS architecture support
  - Example transceiver PCS layout
  - RX standard PCS functional blocks and support
  - RX standard PCS functional block descriptions
  - RX standard PCS low latency mode
  - RX enhanced PCS functional blocks and support
  - RX 10G PCS functional block descriptions
  - RX enhanced PCS low latency mode
  - RX PCS direct mode
  - RX PCIe GEN3 PCS functional blocks
  - RX PCIe GEN3 PCS functional block descriptions

- TX Datapath
  - Transmitter path definition
  - Transmitter block diagram
  - TX PCS architecture support
  - TX standard PCS functional blocks
  - TX PCS functional block descriptions
  - TX standard PCS low latency mode
  - TX enhanced PCS functional blocks

  - TX 10G functional PCS block descriptions
  - TX enhanced PCS low latency mode
  - TX PCS direct mode
  - TX PCIe Gen3 PCS functional blocks
  - TX PCIe Gen3 PCS functional block descriptions
  - TX polarity inversion
  - Transmitter simplified block diagram
  - Transmitter PMA functional blocks
  - Which blocks/configuration do I need?

- Clocking
  - Transceiver clocking
  - Receive path clock generation and example
  - Transmit path clock generation and example
  - ATX PLLs
  - Fractional PLLs
  - CMU PLLs
  - Local CGB
  - Master CGB
  - Input reference clock sources
  - Input reference clock pins
  - Reference clock network
  - PLL cascading
  - RX pins
  - FPGA fabric clocks

- Reset
  - Transceiver reset
  - Transceiver reset control signals

- Building a Arria 10 PHY layer
  - Introduction
  - Aria 10 PHY layer implementation diagram
  - Transceiver design flow
  - IP parameter editors
  - IP output files for compilation
  - PHY IP output files for simulation
  - Using Qsys to build system references
  - Transceiver PHY IP cores
  - Available PHY IP cores
  - Arria 10 native PHY IP core
  - Native PHY IP interfaces
  - Primary clock signals
  - Parallel data interfaces
  - Parallel data interface bit assignment
  - PCS/PMA control and status interface
  - Serial interface
  - Reset control and status interfaces
  - Transceiver PLL IP

- Steps to configuring transceiver PLL IP
- Transceiver PLL IP parameters
- ATX PLL IP parameter editor
- fPLL IP parameter editor
- CMU PLL parameter editor
- Transceiver PLL clock signals
- Transceiver PLL status/control signals
- Transceiver PHY reset controller IP core
- Transceiver PHY reset controller parameter editor
- Transceiver PHY reset controller signals
- Interconnecting the transceiver IP cores
- External transceiver IP core connections

❖ **Lab #1: Configuring Arria 10 Transceiver IP Cores**

Day #2

❖ **Link Bring-Up**

- Setting Static Analog Parameters
  - RX buffer analog SI features
  - CTLE
  - DFE
  - Adaptive parametric tuning engine
  - TX buffer analog SI features
  - Setting static Analog parameters

- Link Analysis & Simulation using JNEye Tool
  - Transceiver link simulation
  - Altera JNEye technology
  - JNEye overview
  - JNEye user interface and correlations
  - JNEye device and link component support
  - Simulation modes in JNEye tool
  - JNEye link simulation
  - Automatic link optimization and adaptation

- Transceiver Toolkit
  - Quartus Prime transceiver toolkit
  - Transceiver toolkit GUI
  - Features overview
  - Auto sweep
  - EyeQ
  - EyeQ heat display

- Enabling transceiver Toolkit support
- ADME
- Example user flow
  - Set up board(s)
  - Open transceiver Toolkit
  - Load design
  - Link hardware resources
  - Identify channels
  - Run tests
- BER reports
- Manual PMA control

❖ **Lab #2: Using the Transceiver Toolkit**

❖ **Transceiver Reconfiguration**

- Introduction
  - What is transceiver reconfiguration?
  - Transceiver reconfiguration uses
  - So I have to employ transceiver reconfiguration?
  - Reconfiguration features, tools and concepts overview
  - Reconfiguration interface
  - Arbitration
  - Configuration files
  - Selecting configuration files (native PHY)
  - Reconfiguration profiles
  - Adding reconfiguration profiles (native PHY)
  - Embedded reconfiguration streamer
  - Transceiver reconfiguration flow

- Performing Transceiver Reconfiguration
  - Performing transceiver reconfiguration
    - Turning on transceiver reconfiguration
    - Connect reconfiguration interface to master
    - Place channels/PLLs in reset
    - Perform Avalon-MM transactions
    - Recalibrate channels and PLLs
    - Release resets

- Transceiver Reconfiguration Examples
  - Calibration overview
  - Calibration register controls
  - Example arbitration registers
  - PMA reconfiguration
  - Configurable PMA settings
  - Example PMA register addresses
  - Analog settings in configuration files
  - Channel and PLL reconfiguration overview

- Steps for channel and PLL reconfiguration
  - Configure the native PHY and transceiver PLL for base instance(s)
  - Configure the native PHY and transceiver PLL for modified instance(s)
  - Use reconfiguration profiles and a single .QSYS file for base and each modification
  - Use separate .QSYS file for each base and modified instance
- Using IP guided reconfiguration flows
- Unsupported reconfiguration

❖ **Lab #3: Transceiver Reconfiguration Profiles**

❖ **Transceiver Design Best Practices**

- Resource Optimization
  - Choosing the best TX PLL (ATX PLL/fPLL/CMU PLL)
  - Merging TX PLLs
  - Why is understanding clocking important?
  - Transceiver clocking
  - Reference clocks
  - Reference clock pin recommendations
  - Internal clocking (TX clock network x1/x6/xN)
  - PLL feedback compensation path bonding
  - GT clock network
  - Native PHY IP channel clocks
  - Native PHY FPGA-transceiver interface clocks
  - Sharing FPGA-Transceiver clocks
  - Additional FPGA clocking
  - Channel placement guidelines
  - Introducing the BluePrint Platform Designer
  - Manual placement restrictions
  - Non-bonded channel placement restrictions
  - GT transceiver bank layout
  - Example GT triplet configurations
  - PMA vs PMA and PCS bonding
  - x6/xN vs. PLL feedback compensation PMA bonding
  - PMA and PCS bonding
  - Channel merging

- Planning Reset Control
  - Reset solutions review
  - When is transceiver resetting required?
  - Using the reset controller IP
  - Possible additional reset connection

- Debugging
  - Loopback
  - Loopback types

- PHY IP Versions
- Pin Connection Guidelines
    - Pin connection example (RREF pin)