HandsOn Training

Intel® FPGA Technical Training

Achieving Timing Closure in Intel FPGAs

Course Description

This course provides all necessary theoretical and practical know-how to analyze and fix timing failures for variety use cases in Intel FPGAs. In addition, the course goes into great depth and touches upon writing timing constraints for source synchronous high speed interfaces such as SDR and DDR.

The course goes into great depth and touches upon every aspect of timing failures due to setup and hold negative slack, I/O input/output delays, reset issues, high fanout, global clock networks, over constrained design, as well as timing exceptions.

The course begins with SDC and timing reports review to highlight which constraints and reports should be written and generated, and when to use each. Then timing closure recommended methodology is discussed with various Quartus Prime tools and advanced settings.

The course continues with an in depth solutions for various timing failures use cases such as too many logic levels, high fanout, confliction SDC assignments, conflicting location assignments, tight timing requirements, clock crossing, and clock skew.

The course ends with how to write and apply timing constraints for source synchronous interfaces such as SDR and DDR, feedback designs, and LVDS timing analysis.

The course covers also the Intel FPGAs clocking resources such as GCLK, RCLK, and PCLK, their features and when to use each.

Timing exceptions are also covered in details (multicycle, false path, clock groups).

The course combines 50% theory with 50% practical work in every meeting.

Course Duration

3 days

Goals

1. Understand TimeQuest reports and when to use each
2. Writing correct SDC constraints
3. Efficiently use timing exceptions in SDC
4. Become familiar with the recommended timing closure methodology
5. Analyze and fix various timing problems
6. Use efficiently the chip planner, TimeQuest, RTL and Technology view for advanced timing analysis
7. Properly constrain and analyze source synchronous interfaces such as SDR and DDR
8. Properly constrain feedback designs
9. Properly constrain LVDS designs
10. Efficiently use the Design Space Explorer tool

Intended Users

Hardware engineers who develop FPGAs and would like to enhance their skills, in order to

fix and solve timing problems in their projects, and acquire better expertise with TimeQuest, and be able to write constraints for advanced interfaces.

Previous Knowledge

FPGA design, VHDL/Verilog, TimeQuest basic knowledge, Quartus II/Prime

Course Material

1. Synthesizer and Place & Route: Quartus Prime
2. Course book (including labs)

Table of Contents

Day #1

❖ Recommended Methodology for Timing Closure

- Setting expectations
- Timing failure analysis flow
- Working with messages
- Common timing constraint issues
- Effect of incorrect timing constraints
- Design assistant
- Timing optimization advisor
- Global and individual speed optimizations
- Physical synthesis types
- Asynchronous control signals and pipelining
- Timing driven compilation (TDC)
- Optimize hold timing
- I/O optimizations
- Report timing approaches
- Evaluate results
- Using the chip planner
- Cross-probe from TimeQuest
- Shows delays and physical routing
- Viewing routing congestion
- Viewing high-speed and low-power tiles

❖ Analyzing & Solving Timing Failures Part I

- Too many logic levels
  - Using the technology map viewer
  - Logic levels in TimeQuest report
- Solutions for too many logic levels
  - Pipeline registers
  - Efficient HDL coding style
  - If-else recommendations
  - Other HDL issues to check
- High fanout
  - High fanout problems
  - Verifying high fanout signals
  - TimeQuest path analysis
- Solutions for high fanout signals
  - Options in advanced fitter settings
  - Analyzing global signal usage
  - Manually promote signals to global resources
  - MAX_FANOUT constraint
  - Manual duplication in assignment editor
  - Manual logic duplication in source code

❖ **Lab#2:** Analyze & solving timing failures using recommended methodology and Quartus Prime tools

Day #2

❖ Analyzing & Solving Timing Failures Part II

- Conflicting physical constraints
  - Reasons for conflicting physical constraints
  - Verify locations in Chip Planner
  - Understanding physical requirements
  - Viewing location constraints in TimeQuest
- Solutions for conflicting assignments
- Tight timing
  - Tight timing requirements
  - Output I/O failing example
- Solutions for tight timing requirements
  - Shifting launch clock
  - Path multicycle
  - PLL clock feedback modes for timing closure
- Clock crossing failures
  - Clock crossing timing failures
- Solutions for clock crossing timing failures
  - Cut paths where appropriate
  - Ensure correct edge analysis in TimeQuest
- Clock skew
  - Clock skew in TimeQuest
  - Different clock network types
- Solutions for clock skew

❖ Understanding Device Clocking Resources

- Timing closure & clocking resources
- Hierarchical clocking resources
- Global clocks (GCLK)
- Regional clocks (RCLK)
- Peripheral clocks (PCLK)
- Section clocks (SCLK)
- PLL
- Clock control blocks
- Utilizing global routing resources
- Tradeoffs when using clock buffer
- Resets and global networks

❖ The Fitter, Seeds & DSE

- Fitter settings per architecture
- Seeds and seed sweeping
- The “Magic” seed
- Seed sweep: monitoring a change
- Design Space Explorer (DSE)
- Exploration spaces
- Recommendations using DSE

- **Over-Constraining**
  - How much to over-constrain?
  - Over-constrain only outside of timing analysis
  - Over-constrain specific “critical” paths
  - Over-constraining clock domains
  - Clock uncertainty in TimeQuest
  - Fitter effort options

- **Lab #3:** Fixing Advanced Timing Failures
- **Lab #4:** Timing optimization using PLLs

Day #3

- **Constraining Source Synchronous Interfaces (SDR, DDR)**
  - Source synchronous interfaces overview
    - SDR center aligned clock
    - SDR edge aligned clock
    - Data captured on same edge
    - Data captured on opposite edge
  - SDR input interface constraints
    - Virtual clocks
    - Direct clocking: center aligned data
    - PLL clocking: center aligned data
    - PLL clocking: edge aligned data
  - Data input timing constraints
    - Tco relative to input & output clock
    - Input delay: setup/hold provided
    - Input delay: center aligned
    - Input delay: edge aligned
    - Specification provides skew
  - SDR output interface constraints
    - Common data and output clock
    - PLL generated clock output
    - DDIO registers
    - Data output timing constraints
    - Skew output constraints
    - Output clock false path
    - Edge aligned output multicycle exception
    - DDIO output false path exception
    - SDR analysis in TimeQuest
  - Source synchronous DDR interfaces
    - Double data rate complexities

        - DDR input and output logic
    - DDR input interface constraints
        - Input clock 90o phase shift
        - Setting DDR input delay constraints
    - Timing exceptions for DDR inputs
        - Same edge transfer
        - Opposite edge transfer
        - Using tSU/tH requirements
    - DDR output interface constraints
        - PLL generated clock output
        - Toggling clock output register
        - Setting output delay constraints
        - Timing exceptions for DDR outputs
        - Same edge transfers
        - Opposite edge transfers
        - Output clock false path
        - Output constraints using skew
    - DDR analysis
        - Output rising-edge setup/hold timing reports

- **Lab #5:** Source Synchronous Interfaces: Single Data Rate
- **Lab #6:** Source Synchronous Interfaces: Double Data Rate

- **Constraining Feedback Designs & LVDS**
    - Clock feedback
        - Required constraints
        - Clock feedback example
    - Data feedback
        - Required constraints
        - Data feedback example
        - Combined feedback techniques
    - LVDS hardware
    - LVDS transmitter
    - Transmitter report
    - Transmitter channel-to-channel skew (TCCS)
    - LVDS receiver
    - Dynamic Phase Alignment (DPA)
    - Non-DPA interface
    - Dedicated SERDES analysis (non-DPA)
    - Key LVDS specifications
        - Time unit interval (TUI)
        - Receiver sampling window (SW)
        - Transmitter channel-to-channel skew (TCCS)
        - Receiver channel-to-channel skew (RCCS)
        - Receiver skew margin (RSKM)
        - LVDS equation
        - Three ways to use RSKM
        - Constraining for link success example
    - Data receiver modes

- DPA/soft-CDR mode analysis

❖ **Lab #7:** Constrain Feedback designs for clock and data
❖ **Lab #8:** Constrain LVDS receiver and analyze in TimeQuest

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