



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

altera™ solution acceleration partner

Designing with Quartus Prime Pro

Course Description

This 3-days training provides all necessary information to start designing with Altera FPGAs using Quartus Prime Pro software.

The course starts with an overview of the Quartus Prime design software features, Quartus Prime projects types and management, design methodology, and using IP cores from the IP catalogue.

Various system design entry tools such as Platform system integration tool, state machine editor, memory editor, oneAPI SYCL HLS, Altera FPGA AI Suite, and DSP Builder are also introduced in high level.

The course continues with the Quartus Prime compilation flow, working with messages, viewing compilation reports, RTL and technology views, state machine viewer, and how to use the chip planner tool.

The course also touches upon simulation, synthesis and Place & Route settings as well as, assignment editor, optimizations, design assistant and scripting methods to automate design tasks.

Next, the I/O planning with the pin planner & Interface Planner tool is introduced and how to use it efficiently in complex designs.

The training continues by introducing Platform Designer, incremental optimization, and block-based design methodologies. Then Timing Analyzer tool introduced to enable writing SDC files and analyze timing.

The course ends with tips how to convert design from non-Altera to Altera FPGA.

The course includes extensive practical work. The practical labs cover all of the theory.

Each attendee receives an official certificate from Altera (Exam must be passed)



When innovation meets expertise...



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

Course Duration

3 Days

Goals

1. Create a new Quartus Prime Pro project
2. Choose supported design entry methods
3. Compile a design into a programmable logic device
4. Locate resulting compilation information
5. Create design constraints (assignments & settings)
6. Manage I/O and interfaces assignments
7. Use the Interface Planner for complex designs
8. Be familiar with Timing Analyzer new features for timing analysis
9. Automate your design using scripting
10. Convert a non-Altera design to Altera FPGA

Intended Users

Digital hardware engineers that would like to design with Altera FPGAs.

Altera FPGA designers that would like to migrate from Quartus Prime Standard to Quartus Prime Pro.

Prerequisites

1. FPGA design
2. HDL experience
3. FPGA architecture understanding

Course Material

1. Quartus Prime Pro
2. Questa
3. Course book
4. Lab handbook



When innovation meets expertise...

Table of Contents

Day #1

❖ Introduction to the GUI

- Basics of Altera Quartus Prime design software
- Quartus editions and devices support
- New features and enhancements
- Then Quartus Prime Pro software
- Default operating environment
- Main tool bar
- Tcl console window
- Migration from Standard to Pro edition

❖ Altera FPGA Compilation Flow

- Compilation flow overview
- What is synthesis?
- Fitter checkpoint and snapshot
- Fitter stages
- Compilation tasks
- Compilation dashboard

❖ Design Entry

- Design entry file types supported
- Inferring resources in Altera FPGAs
- What is Adaptive Logic Module?
- What is Adaptive Look-Up Table?
- Verifying hardware inference from HDL
- How to use templates for inferring resources?
- FPGA IP cores
- IP Base Suite
- Altera FPGA IP
- IP settings
- The State Machine Editor



When innovation meets expertise...

- The Memory Editor
- Using a memory file in IP
- Third-party tools support

❖ **System Design**

- System design entry tools
- System design entry with Platform Designer
- Platform Designer concept and GUI
- Visual Designer Studio
- DSP Builder for Altera FPGAs
- oneAPI SYCL HLS FPGA Development Flow
- Altera FPGA AI Suite

❖ **Simulation**

- Project testbenches
- Modify project settings
- Generate simulation files
- Run simulation

❖ **Settings & Assignments**

- Settings dialog box
- Compiler settings
- Software settings file
- Settings and assignments priority
- Revisions
- Assignment editor
- Updating the .qsf file

❖ **Quartus Software-Physical Layout**

- Pin Planner tool
- Assigning pin locations
- Pin location results
- Pin legend and pin planner views
- Tasks and report windows



When innovation meets expertise...



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

- Reserved and unused I/O pins
- Chip planner tool
- Logic Lock Regions
- Merging Logic Lock regions
- The Interface Planner
- Create and synthesize representative design
- Open and initialize Interface Planner
- Check imported assignments and update plan
- Create interface plan
- Validate plan
- Export constraints
- Source into project and compile

❖ **Netlist Viewers & Cross Probing**

- Various RTL Analyzer viewers
 - Netlist viewers
 - Schematic view
 - Technology map viewer
 - Other features
 - Cross probing
 - Path located in Chip Planner
-
- **Lab #1: Create a project with IPs**
 - **Lab #2: Create revision and make design constraints**
 - **Lab #3: Locate information in the compilation report and explore cross probing capabilities**



When innovation meets expertise...

Day #2

❖ Early Design Planning Using Interface Planner

- FPGA implementation phases
- The need for interface planning
- Interface planning before
- Problem: periphery interfaces are complex
- Previous flow: Pin Planner and Assignment Editor
- Better solution: interface-based assignment
- Introducing the Interface Planner
- Interface Planner in the compilation flow
- Interface Planner usage flow
 - Create and synthesize representative design
 - Sources of initial design
 - Using a design from the design store
 - Virtual pins
 - Open and initialize Interface Planner
 - Initialization summary report
 - Check imported assignment and update plan
 - Plan tab chip view – click and drag
 - List available locations
 - Chip view results
 - Cross-highlight placed elements
 - Continuous legality syncing
 - Link info
 - Automatic placement
 - Package view results
 - Individual pins
 - Clock network floorplanning
 - Save/Load/Reset Plan
 - Interface Planner reporting
 - Additional reports
 - Validate I/O plan
 - Write out constraints file



When innovation meets expertise...



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

- Source into project & compile
- Board design resources and interface handoff
- Pin Planner vs Interface Planner

- **Lab #4: Migrate a Design and Perform Early Design Planning**

- ❖ **Implementation with Incremental Optimization & Block-Based Design**

- Platform Designer
 - Platform Designer in the FPGA design flow
 - PD advantage: automatic interconnect generation
 - Target PD applications
 - Features
 - Design reuse possibilities
 - Project association
 - The PD GUI
 - Platform Designer vs Platform Designer Standard
 - Additional Platform Designer Pro features
- Incremental Optimization
 - Fitter stages and Incremental Optimization overview
 - Checkpoints and snapshots
 - Early placement
 - Per-stage compilation benefits
 - Using the multi-stage fitter
 - Per-stage fitter reports contents
 - Incremental Optimization features availability
 - Per-stage fitter reports
 - Per-stage timing analysis
 - Timing analyzer launch from compilation dashboard
 - Plan checkpoint
 - Place checkpoint
 - Using post-place timing analysis
 - Scenarios for using post-place timing analysis
 - Route checkpoint
- Block-Based Design: Partitions & Logic Lock regions
 - What are user-defined design partitions?



When innovation meets expertise...



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

- Design partitions example
- What can be a partition?
- Core vs periphery partitions
- Resource classification
- Setting design entities as partitions
- Design partitions window
- Design partition planner
- No optimizations across boundaries for synthesis
- What are Logic Lock regions?
- Logic Lock regions in Chip Planner
- Logic Lock regions window
- Logic Lock regions assignment syntax
- Merging Logic Lock regions
- Non-rectangular regions in the QSF file
- Hierarchical region constraints
- Overlapping regions with different assigned instances
- Routing regions
- Routing type
- Logic Lock region comparison: Standard vs Pro
- Incremental Block-Based Design
 - Example uses
 - Top-down design model flow
 - Understanding preservation level
 - Partitin Netlist types
 - Compilation flow
 - Empty assignment
 - Empty vs final partitions
 - Bringing Empty partitions back
 - Using Incremental Block-Based compilation
 - Creating black box wrapper files
 - Quick periphery planning
- Design block reuse
 - Reuse design flows: core reuse
 - Reuse design flows: root partition reuse
 - Developer project flows



When innovation meets expertise...

- Export partition
- Files to hand-off
- Design partitioning
- Integrate reused core partition
- Periphery reuse
- Compile & create core logic
- Partial reconfiguration
 - What is partial reconfiguration?
 - Partial reconfiguration applications
 - Physical interfaces for partial reconfiguration
 - Partial reconfiguration considerations
- **Lab #5: Use Block-Based Design Methodology**

Day #3

❖ Timing Analysis

- Specify SDC file(s)
- Timing Analyzer
- Timing Analyzer GUI
- Basic steps for using timing analyzer
- Generate timing netlist
- Constrain directly in console
- Constraining
- Generate timing reports
- Advanced clock pessimism
- Pessimism removal background
- Advanced clock pessimism removed
- EOL and PSIJ
- Report clock waveforms
- Clock Domain Crossing (CDC) viewer
- Live filtering
- CDC viewer details
- **Lab #6: Examine the New Features in the Timing Analyzer**

❖ JTAG Debugging Tools

- Signal Tap Embedded Logic Analyzer
 - When to use Signal Tap ELA?
 - Signal Tap resource utilization
 - Feature overview
 - Methods of adding Signal Tap ELA
 - Signal Tap logic analyzer window
 - Signal configuration
 - Remote debugging
 - Data files for analysis
 - Scripting support
- In System Sources & Probes (ISSP)
 - Features overview
 - When to use Sources and Probes?
 - Create Sources and Probes FPGA IP
 - ISSP editor
- In System Memory Content Editor (ISMCE)
 - When to use ISMCE?
 - Steps to using ISMCE
 - In-system editor options

❖ Quartus Scripting

- Quartus Prime command-line support
- Benefits of command-line executables
- Options and reports
- Typical design flow
- Integrated into the GUI
- Typical use scenarios
- Getting help – command line options
- Qhelp utility
- Tcl for expanded control
- Other ways to use Tcl control
- Tcl packages
- Using ::quartus::flow to fully automate your flow
- Assignment files
- Using Tcl as part of your QSF file



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

- Example scenario
- Assignment precedence
- Writing settings files
- Archive or restore a project example
- Fit a design using multiple seeds example
- Platform designer executables
- Simulation script generation

- **Lab #7: Scripting & Automating**

❖ **Design Conversion Tips**

- Capture golden test vectors
- Convert resources
- Verify functionality

- **Lab #8: Convert a non-Altera design to Altera design and simulate the design to ensure latency and functionality is preserved**



When innovation meets expertise...