



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

altera™ solution acceleration partner

Designing with Agilex 5 SoC

Course Description

The training starts by introducing the Agilex 5 family and its architecture. Then the Hyperflex architecture and how to use it efficiently is discussed in details. The Quartus Prime Pro advanced features that support Agilex 5 are introduced along with practical hands-on labs.

In the second day the training continues with the high-speed memory interfaces, high speed serial interfaces (GTS transceivers and various IPs), and the MIPI interface with CSI2/DSI2.

In the third day the Hardware Processor System (HPS) is introduced along with its peripherals, interfaces, Network on Chip (NoC), and Cortex-A76 & Cortex-A55 architecture and capabilities. This part covers also the boot flow in details, and how to generate the first and second bootloaders (FSBL, SSBL).

In the fourth day the Agilex 5 configuration schemes are discussed in details including the Remote System Update (RSU) design flow. In addition, the Agilex 5 security features are discussed in details including the Secure Device Manager (SDM) and the secure boot flow.

In the fifth day the Agilex 5 DSP with Tensor block architecture is introduced. Then the deployment of AI IP design flow is discussed in details.

Each attendee receives an official certificate from Altera (Exam must be passed)



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Course Duration

5 days

Goals

- Become familiar with the Agilex 5 capabilities
- Use the Hyperflex gen2 architecture with Quartus Prime Pro tools to accelerate performance and fix timing issues
- Implement high-speed external memories interfaces, serial protocols, and video solutions
- Become familiar with the Agilex 5 HPS using Arm Cortex-A76 and Cortex-A55
- Implement SoC design with Quartus Platform Designer
- Become familiar with Agilex 5 security features, and the secure boot flow from power up, as well as run-time security features
- Become familiar with Agilex 5 support for functional safety applications
- Use the AI Suite to deploy AI IP that utilized the DSP Tensor blocks

Intended Users

FPGA designers who would like to start developing with Altera Agilex 5 SoC.

Prerequisites

1. FPGA design experience
2. Quartus Prime Pro
3. Platform Designer tool

Course Material

1. Course book
2. Labs handbook with lab files
3. Quartus Prime Pro
4. Questa



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Day #1

❖ Introduction to Agilex 5 FPGA Family

- Family overview
- Agilex 5 main features
- Agilex 5 ALM and modes
- Agilex 5 LC and LE
- Agilex 5 transceivers
- Agilex 5 on-chip memory

❖ Agilex 5 Hyperflex Architecture

- 2nd generation Hyperflex FPGA architecture performance benefits
- Conventional vs Hyperflex architecture
- 2nd generation Hyperflex FPGA architecture in details
- High-Performance: Hyper-Retiming
- Eliminating barriers to Hyper-Retiming
- High-Performance: Hyper-Pipelining
- High-Performance: Hyper-Optimization
- Using Fast-Forward with Hyper-Optimization
- Pre-Computation technique
- Power consumption optimization
- Analyzing critical chains

❖ Quartus Prime Pro Edition Design Software for Agilex 5

- Agilex 5 features support in Quartus Prime Pro
- Hyperflex compilation flow features
- Fast Forward compile tool & reports
- Power & Thermal Calculator (PTC)
- Design Assistant tool
- System-Level Debug
- Enhanced Visualizations
- Incremental optimization



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- **Lab #1: Create a project with a complete design flow**
- **Lab #2: Fix timing issues with Hyper-optimizations**
- **Lab #3: Calculate power consumption with PTC tool**

Day #2

❖ **High-Speed External Memory Interfaces in Agilex 5**

- External memory support in Agilex 5
- DDR 5 advantages
- Agilex 5 Hard Memory Controller (HMC) architecture and features
- Agilex 5 High-Speed I/O (HSIO) architecture
- ECC support
- Agilex 5 EMIF IP design flow & checklist
- Configuring & generating the IP
- Simulating memory IP
- Validating the IP with the Performance Monitor & Test Engine IP
- EMIF debugging
- **Lab #4: Implement high-speed interface for DDR memory**

❖ **Implementing High-Speed Serial Interfaces in Agilex 5**

- Introduction to Agilex 5 GTS transceiver
- Transceivers architecture, capabilities and performance
- Implementing Forward Error Correction (FEC)
- PCIe architecture
- Scalable scatter-gather DMA IP overview
- Transceiver supported tools (transceiver toolkit, advanced link analyzer, PTC, transmitter equalization tool)
- **Lab #5: Implement PCIe Gen 4.0 and use the transceiver tools to verify the signal quality**



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❖ **Implementing Ethernet & TSN (Time Sensitive Network) in Agilex 5**

- Ethernet support in Agilex 5 FPGAs
- Ethernet hard & soft IPs
- Ethernet TSN support
- **Lab #6: Implement 10 GbE interface**

❖ **Video Solutions with Agilex 5**

- MIPI D-PHY
- CSI2/DSI2
- Combining high-speed Ethernet, memory controllers, PCIe
- Video processing & connectivity IP portfolio

Day #3

❖ **Agilex 5 Hard Processor Subsystem (HPS)**

- Introduction to SoC FPGA design
- HPS in details (including NoC and peripherals)
- Arm Cortex-A76 and Cortex-A55 architecture in details
- Using the SoC FPGA in Quartus Prime software with Platform Designer
- Boot stages and the Secure Device Manager (SDM)
- HPS pin multiplexing
- Power management
- Configuring the HPS component in Platform Designer
- Simulating the HPS component
- **Lab #7: Using the SoC FPGA in Quartus Prime software**
- **Lab #8: Generating the First & Second Bootloaders**



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Day #4

❖ **Agilex 5 Configuration Overview**

- Device configuration & SDM in Agilex 5 and SoC
- Agilex 5 configuration overview
- Configuration and related signals
- SDM block diagram
- Updating the SDM firmware
- Configuration timing diagram
- Recoverable and unrecoverable configuration errors
- Configuration flow
- Configuration pins
- Specifying configuration scheme
- Quartus Fitter report and SDM I/O pin reporting
- Agilex 5 dedicated configuration pins

❖ **Agilex 5 Configuration Schemes**

- Avalon-ST configuration
- Output file types
- Programming file generator
- AS configuration
- Selecting QSPI ownership
- Configuration data widths and required signals
- Components and design flow using AS configuration scheme
- Agilex 5 configuration data width and device pins
- JTAG configuration scheme
- Configuration via protocol (CvP)
- CvP core image update
- CvP topologies
- Partial reconfiguration design flow



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❖ **Agilex 5 Remote System Update (RSU)**

- RSU introduction
- Typical RSU process
- Agilex 5 RSU components
- RSU configuration sequences
- RSU functions for non-HPS

❖ **Agilex 5 Security Features**

- Why do you need security in your FPGA?
- Agilex 5 security features overview
- Agilex 5 security features in details (including HPS security)
- Bitstream authentication & encryption
- Advanced security features (provisioning, attestation, crypto services)
- Physical anti-tamper
- **Lab #9: Experience with Partial Reconfiguration flow**
- **Lab #10: Apply security features to protect the design**

❖ **Functional Safety on Agilex 5**

- What is Functional Safety (FuSa)?
- Why Agilex 5 FPGA for FuSa?
- Altera offering for FuSa



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Day #5

❖ **Agilex 5 Enhanced DSP with AI Tensor Block**

- Variable-precision DSP in Agilex 3 and SoCs C-series
- New tensor mode
- Fixed point arithmetic mode
- Independent complex multiplier
- Systolic FIR mode
- Floating point arithmetic mode
- Differences between flushed, extended, and Bfloat formats
- Complex multiplication
- Tensor mode block diagram
- Tensor floating point mode
- Tensor fixed point mode
- Tensor accumulation mode
- Methods for preloading the weights

❖ **Deploy AI IP Design Flow in Agilex 5**

- The role of FPGA in AI
- Agilex 5 DSP with AI Tensor block
- OpenVINO Toolkit & AI suite for Agilex 5
- Compilation & IP creation flow
- Reference design examples and new features
- **Lab #11:** Deploy AI IP in Agilex 5 (complete flow)