



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

altera™ solution acceleration partner

Clock Domain Crossing Considerations

Course Description

As FPGA designs grow in complexity, the use of multiple asynchronous clock domains has become a standard necessity. However, improper handling of signals crossing these boundaries is the #1 cause of intermittent, "impossible-to-debug" hardware failures.

This 2-days course provides a comprehensive technical deep-dive into the challenges of Clock Domain Crossing (CDC). We go beyond simple synchronization to explore advanced protocols, structural verification, and the mathematics of Metastability. Engineers will learn how to design robust interfaces that ensure deterministic behavior across independent clock regions.

The course provides the "how" to constraint such domains and analyze them in Quartus Prime Pro either in QSF and SDC files.

Course Duration

2 days

Goals

- **The Physics of Failure:** Understand **Metastability**, Mean Time Between Failures (MTBF), and why standard Static Timing Analysis (STA) cannot catch CDC issues
- **Synchronization Patterns:** Master single-bit vs. multi-bit crossing techniques, including Gray coding and handshaking
- **Structural Verification:** Learn to use the Quartus CDC Viewer to identify unmasked paths
- **Asynchronous FIFOs:** Deep-dive into the architecture of dual-clock FIFOs, pointer synchronization, and full/empty logic



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- **Reset Synchronization:** How to handle asynchronous reset assertion and synchronous de-assertion to prevent "glitch" states

Intended Users

FPGA designers, verification engineers who design with multi-clock domains with Altera FPGAs, and would like to understand all design considerations, constraints, analysis and when to use each solution.

Prerequisites

- Altera FPGAs architecture
- Quartus Prime Pro software
- Questa

Course Material

1. Course book
2. Lab's handbook and lab files
3. Questa
4. Quartus Prime Pro



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Table of Contents

Day #1

❖ Synchronization Circuits

• Multiple Clock Domains

- Why synchronous design?
- Synchronization circuits introduction
- Setup and Hold time violations
- Metastability effects
- MTBF Calculations: Understanding the probability of failure in 7nm/5nm processes
- Metastability problem
- Unique characteristics of MTBF

• Single-Bit & Control Signal Crossing Synchronizers

- Synchronizer definition
- Two FF synchronizer
- Three FF synchronizer
- Not recommended synchronization circuit
- Proper use of a synchronizer
- Unregistered signals sent across a CDC boundary
- Registered signals sent across a CDC boundary
- Passing a fast control signal
- Wide enable signal detection
- Narrow enable signal regeneration
- Level alternation scheme
- Synchronizing fast control signals into slow clock domains
- Sampling long CDC pulse
- Open loop solution and considerations
- Closed loop solution and considerations

• Multi-Bit Data & Bus Synchronizers

- Passing multiple signals between clock domains
- Capturing a bus example
- Passing multiple control signals between clock domains
- Synchronized pulse generation logic
- Send-receive toggle-pulse generation
- Multicycle path and FSM solutions
- MCP with feedback
- MCP with acknowledge feedback



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- **Lab #1: Implement fast-to-slow and slow-to-fast synchronizers**
- **Lab #2: Implement and verifying a 4-phase handshake controller**

Day #2

- **Asynchronous FIFO as a Synchronizer**
 - Asynchronous FIFO architecture
 - FIFO pointers implemented as binary counters vs gray code counters
 - Generating “safe” Full and Empty flags
 - Gray code incrementor design for high speed
 - 1-deep 2-register FIFO synchronizer
 - Design tips
- **Design Partitioning for Synchronization**
 - Synthesis of a multiple clock system
 - Where to synchronize?
 - Guidelines for design partitioning
 - Partitioning with multi-cycle path
- **Reset Synchronizers**
 - Synchronous and asynchronous reset differences
 - When to use synchronous and asynchronous reset
 - Asynchronous reset problem
 - Reset synchronizer
 - Non-coordinated reset removal
 - Sequenced coordination of reset removal
- **Metastability Constraints & Analysis in Quartus Prime Pro**
 - Managing metastability with Quartus Prime Pro
 - Metastability analysis in Quartus Prime Pro
 - Identifying synchronizers for metastability analysis
 - Timing constraints for CDC paths
 - Altera Parameterizable macros
 - CDC viewer reporting tool
 - MTBF reporting in TimeQuest
 - Synchronizer data toggle rate in MTBF calculation
 - False path reporting in TimeQuest
 - MTBF optimization
- **Lab #3: Designing a custom Asynchronous FIFO from scratch in SystemVerilog/VHDL along with reset synchronizers**
- **Lab #4: constraining and running a full CDC structural report on a multi-clock design**



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