



OREN HANDS ON TRAINING & DEVELOPMENT LTD.
20 YAIR ROZENBLUM ST. KFAR SABA 4464601 ISRAEL

altera™ solution acceleration partner

Building Systems with Platform Designer

Course Description

This course will teach you how to quickly build systems for Altera FPGAs using the Platform Designer system-level integration tool.

You will become proficient with Platform Designer and expand your knowledge of the Quartus Prime Pro FPGA design software.

You will learn how to quickly integrate IP and custom logic into a system.

Since Platform Designer makes design reuse easy through standard interfaces, we will examine the Altera Avalon-Memory Mapped and Streaming Interfaces as well as introduce the AMBA AXI interface standard from ARM.

The class provides a significant hands-on component, where you will gain exposure to tool usage as well as system and custom HDL component design.

Each attendee receives an official certificate from Altera (Exam must be passed)

Course Duration

2 days

Goals

1. Build digital systems using the Platform Designer tool
2. Integrate the files generated by Platform Designer into the Quartus Prime Pro design flow
3. Create custom components with Avalon-MM and Avalon-ST interfaces and integrate them into your system
4. Exploit Platform Designer hierarchical capability to add flexibility & scalability to your design
5. Explore the design through various tools and reports



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Intended Users

FPGA engineers who would like to use Platform Designer to build simple & complex systems on chip

Prerequisites

- Altera FPGAs architecture
- Quartus Prime Standard/Pro software
- VHDL/Verilog

Course Material

1. Quartus Prime Pro
2. Course book
3. Lab's handbook and labs files



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Table of Contents

Day #1

❖ Introduction to Platform Designer

- Traditional vs Platform Designer system design
- Target PD applications
- System control
- PD features
- Design re-use possibilities
- PD Pro edition specific features

❖ Using Platform Designer

- Platform designer user interface
- .qsys file
- What is Board-Aware design?
- The PD GUI in details
- IP catalog and board tab
- Hierarchical system design with packed subsystems: .qcp files
- Parameter editor
- Presets
- Creating new custom presets
- Component interfaces
- Connections column
- Exporting interfaces
- Conduit interfaces
- Presets for board-aware flow
- Creating a board file
- Exported interfaces
- Clock interfaces



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- Reset interfaces
- Memory-mapped addressing
- Enhanced address map
- Hierarchy tab
- Additional useful features
- System filtering
- Live filtering of system view
- Advanced filtering
- System generation
- Messages
- PD output files
- Integrate PD into design flow

❖ Platform Designer Interconnect

- PD interconnect architecture
- Supported standard interfaces
- Packetized data transfers
- Network-on-chip architecture
- Embedded components arbitration logic
- Adjusting arbitration priority
- Interconnect visualization

❖ Key Off-The-Shelf IP

- Basic IP components
- Streaming IP components
- Memory IP components
- DMA IP components
- Tri-state IP components
- Memory mapped bridge IP components
- High-speed interface IP components
- Processor IP components

- **Lab #1: Build a Video Datapath Hardware System Design Part I**

Day #2

❖ **Creating Custom Components**

- Key elements for component creation
- Adding existing IP variants
- Add/create new subsystem
- Export system-level HDL parameters
- .ip file use and editing
- Component instantiation and implementation types

❖ **Standard Interfaces & Signaling**

- Standard interfaces in custom components
- Clock interface signals
- Reset interface signals
- Avalon streaming interface concepts
- Avalon streaming interface signals
- Avalon streaming interface properties
- Avalon streaming Credit interface & signals
- Avalon Memory-Mapped concepts
- Basic Avalon Memory-Mapped host signals
- Basic Avalon Memory-Mapped agent signals
- Memory-Mapped transfer properties
- Default addressing
- Dynamic bus sizing
- byteenable signaling
- pipelined transfer latency options
- AXI review
- AXI read and write transactions

❖ **Custom Components Design Methodology**

- Bringing existing designs into platform designer
- Example custom component use in system



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- HDL implementation of component interfaces

❖ Platform Designer Integration

- Component editor
 - Auto-port naming convention
 - Individual signal settings
 - _hw.tcl file
 - Add component to PD system
 - Edit component options in place
 - Multiple versions of same component
 - Component editor template
 - Configuring a Blackbox generic
 - Configuring an HDL generic
 - Component file management recommendation
-
- **Lab #2: Build a Video Datapath Hardware System Design Part II**



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