altera
An Intel Company

Designing with Agilex 5 SoC

Course Description

This 4-days course provides all necessary know-how for hardware engineers that would like to design with Agilex 5 SoC FPGA.
The training adds a rich set of hands-on labs to provide the attendee to experience with the device either on EVB or just with FPGA design software.

Altera Agilex 5 Family provides midrange FPGAs offering world-class features and capabilities that address design challenges across various markets. Agilex 5 FPGAs optimized for applications requiring high performance, lower power, and smaller form factors.

Agilex E-Series is optimized for power and size, while Agilex D-series is optimized for performance and power efficiency.

The training starts by introducing the Agilex 5 FPGAs architecture (I/O, DSP, RAM, PLLs, etc.), it's 2nd generation Hyperflex architecture, and the Quartus Prime Pro design software for Agilex 5.

The training continues by teaching how to implement high-speed external memory interfaces, high speed serial interfaces, PCIe and Ethernet (with TSN).

Next, the Hard Processor Subsystem (HPS) is covered with Cortex-A76 and Cortex-A55, along with their peripherals, NoC architecture, design considerations and debug capabilities.

The training ends with the Agilex 5 security features and functional safety.

An optional extension available is the FPGA AI suite for Agilex 5 and the design flow for AI.

Course Duration

4 days (+1 optional)

Goals

1. Become familiar with the Agilex 5 capabilities.
2. Use the Hyperflex gen2 architecture with Quartus Prime Pro tools to accelerate performance and fix timing issues.
3. Implement high speed interfaces such as DDR4/5, PCIe, Video and MIPI, Ethernet and TSN.
4. Use the transceiver toolkit to analyze and debug the signal quality and performance.
5. Become familiar with the Agilex 5 HPS using Arm Cortex-A76 and Cortex-A55
6. Implement SoC design with Quartus Platform Designer.
7. Become familiar with Agilex 5 security features, and the secure boot flow from power up, as well as run-time security features.
8. Become familiar with Agilex 5 support for functional safety applications.
9. Deploy AI IP in Agilex 5 using the OpenVINO toolkit and AI Suite.

Intended Users

FPGA engineers who would like to design with Agilex 5 SoC FPGA family.

Prerequisites

1. VHDL/Verilog language
2. FPGA design experience of at least 3 years
3. Experience with SoC FPGA design

Course Material

1. Course book
2. Lab handbook
3. Trainer solutions to all labs

Table of Contents

Day #1

Day #2

❖ Implementing High-Speed External Memory Interfaces in Agilex 5

- External memory support in Agilex 5
- DDR 5 advantages
- Agilex 5 Hard Memory Controller (HMC) architecture and features
- Agilex 5 High-Speed I/O (HSIO) architecture
- ECC support
- **Lab #1: Implement high-speed interface for DDR memory**

❖ Implementing High-Speed Serial Interfaces in Agilex 5

- Introduction to Agilex 5 GTS transceiver
- Transceivers architecture, capabilities and performance
- Implementing Forward Error Correction (FEC)
- PCIe architecture
- Scalable scatter-gather DMA IP overview
- Transceiver supported tools (transceiver toolkit, advanced link analyzer, PTC, transmitter equalization tool)
- **Lab #2: Implement PCIe Gen 4.0 and use the transceiver tools to verify the signal quality**

❖ Implementing Ethernet & TSN (Time Sensitive Network) in Agilex 5

- Ethernet support in Agilex 5 FPGAs
- Ethernet hard & soft IPs
- Ethernet TSN support
- **Lab #3: Implement 25 GbE interface**

- **Video Solutions with Agilex 5**
  - MIPI D-PHY
  - CSI2/DSI2
  - Combining high-speed Ethernet, memory controllers, PCIe
  - Video processing & connectivity IP portfolio

Day #3

- **Agilex 5 Hard Processor Subsystem (HPS)**
  - Introduction to SoC FPGA design
  - HPS in details (including NoC and peripherals)
  - Arm Cortex-A76 and Cortex-A55 in details
  - Using the SoC FPGA in Quartus Prime software
  - Boot stages and the Secure Device Manager (SDM)
  - **Lab #1:** Using the SoC FPGA in Quartus Prime software

Day #4

- **Agilex 5 Security Features**
  - Why do you need security in your FPGA?
  - Agilex 5 security features overview
  - Agilex 5 security features in details (including HPS security)
  - Bitstream authentication & encryption
  - Advanced security features (provisioning, attestation, crypto services)
  - Physical anti-tamper
  - **Lab #1:** Security design flow to address specific requirements

- **Functional Safety on Agilex 5**
  - What is Functional Safety (FuSa)?
  - Why Agilex 5 FPGA for FuSa?
  - Altera offering for FuSa

Day #5 (Optional)

❖ Deploy AI IP Design Flow in Agilex 5

- The role of FPGA in AI
- Agilex 5 DSP with AI Tensor block
- OpenVINO Toolkit & AI suite for Agilex 5
- **Lab #1:** Deploy AI IP in Agilex 5 (complete flow)