



Designing with i.MX6 Architecture

Course Description

Designing with i.MX6 architecture is a 3 days NXP official course. The course goes into great depth and provides all necessary know-how to develop software for systems based on i.MX6 processor.

The first day starts by overviewing the i.MX6x Family and its Target applications, Device architecture (QuadPlus/Quad/DualPlus/Dual/Dual-Lite/Solo/Solo-Lite/SoloX/SLL/UltraLite/ULL/ULZ), and family roadmap. The course continuous with deep dive training of all i.MX6 internal blocks and accelerators such as memory system and DDR controller (MMDC), USB, SATA, PCI-E, eMMC/SD, NAND controller, Audio subsystem, clocking and reset, and power management unit.

The second day covers the Cortex-A9 MPCore architecture and capabilities, the smart DMA (SDMA), I/O muxing (with IOMUX tool), and GPMI and NAND interface subsystem, 1G Ethernet + IEEE1588, and MIPI display and sensor interface.

The third day covers the boot process (including secured boot with HAB) and boot devices, security features and hardware blocks, Image Processing Unit (IPU), Video Processing Unit (VPU), Graphics Processing Unit (GPU), and HDMI.

Course Duration

3 day

Goals

1. Become familiar with i.MX6 architecture
2. Become familiar with Cortex-A9 MPCore architecture
3. Choose the right DDR device and configure the right mode



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4. Connect efficiently cameras, displays and audio devices/Codecs
5. Design clock, reset and power management strategy
6. Configure the SDMA and load scripts
7. Configure I/Os with IOMUX tool
8. Choose NAND interface and configure ECC with BCH
9. Decide how to Boot and use secure boot with HAB
10. Secure your system with security hardware blocks and TrustZone
11. Encode/Decode video streams with VPU
12. Enhance image processing with IPU
13. Combine 2D and 3D graphics
14. Choose the right embedded board solution

Target Audience

Software engineers that would like developing software and BSP for platforms based on i.MX6 SoC

Prerequisites

- Computer architecture background
- ARM Cortex-A is an advantage but not mandatory
- Experience in developing embedded systems



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Agenda

Main Topics:

- Main features and road map
- i.MX6 series overview
- Device architecture overview
- Memory system and DDR controller
- i.MX6 interfaces overview
- Cortex-A9 MPCore platform overview
- Clocking and reset
- Power management
- Cortex-A9 MPCore architecture and capabilities deep dive
- SDMA
- I/O muxing
- GPMI and NAND interface subsystem
- 1GbE
- MIPI sensor and display
- i.MX6 Boot
- i.MX6 security
- Image Processing Unit (IPU)
- Video Processing Unit (VPU)
- Graphics Processing Unit (GPU)
- Embedded board solutions



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Day #1

❖ Introduction to the i.MX6 architecture

- **i.MX6 Family Roadmap**
 - i.MX6x, i.MX7x, i.MX8x
 - Cortex-A5x series partnership
 - Freescale's product longevity program
- **i.MX6 Market Applications Overview**
 - Platform strategy
 - Smart devices examples
- **i.MX6 Series Overview**
 - One Platform, differentiated products
 - Differentiated features
 - Scalability & compatibility from Solo to Quad core
 - Intelligent integration of multimedia
 - Triple-Play graphics support
 - Quad/Dual/DualLite/Solo/SoloLite/SoloX block diagrams
 - Part number definition and packaging options
 - Development boards
 - Yocto and Android roadmaps
- **Device Architecture Overview**
 - SoC block diagram
 - Cortex-A9 platform
 - Dual and quad core advantages
 - Video & graphics systems
 - Display support and muxing
 - Video encode, decode capabilities
 - Vector graphics, 2D composition engine and OpenGL/openCL GPU engines
- **Memory System & DDR Controller**
 - Multi-Mode DDR Controller (MMDC) main features
 - MMDC block diagram
 - MMDC highlights
 - MMDC control: low power
 - MMDC calibration



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- MMDC configuration examples
 - Low latency and guaranteed bandwidth
 - MMDC configuration in memory map
 - DDR channels and address mapping
 - MMDC modes and basic settings
 - DDR3 DLL OFF mode
 - Two channel interleaving
 - Bus system and QoS
 - DDR arbiter
 - MMDC debug
 - Bus/DDR profiling
 - DDR power saving modes
- **i.MX6 Interfaces**
- Memory & mass storage interfaces
 - SD/eMMC
 - SATA II
 - USB
 - Ethernet controller
 - PCIe 2.0
 - Audio system
 - UART, eCSPI, keypad, one-wire, GPT, PWM, I2C, GPIO
 - Camera interface and displays
- **Introduction to the Cortex-A9 MPCore Architecture**
- Cortex-A9 MPCore platform overview
 - Platform configuration
 - Core configuration
 - L2 Cache configuration
- **i.MX6 Clocking & Reset**
- Clock generation scheme
 - Clock generation deep dive
 - Clock management system block diagram
 - PLL control & status functions
 - Clock Control Module (CCM)
 - Low Power Clock Gating (LPCG)
 - Clock configuration
 - Clock change procedure
 - System Reset Controller (SRC)
 - Power-On reset & power sequencing
 - SRC functional description
 - POR, Cold and Warm reset



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- **i.MX6 Power Management**
 - Power management system
 - Integrated PMU components
 - General Power Controller (GPC)
 - Power-up/down sequence
 - Logic state retention
 - Voltage domain management
 - DVFS examples
 - Standby Leakage Reduction (SLR)
 - System power tree
 - Freescale PF series PMIC (PFUZE)
 - Processor power needs
 - PF0100 overview
 - Low power modes
 - Wake-up events
 - Power saving techniques
 - Temperature monitor
 - Balance high performance and low power
 - Main memory power management
 - ONOFF button support

Day #2

❖ i.MX6 architecture Deep Dive

- **Cortex-A9 MPCore Features & Capabilities**
 - ARM processors overview
 - Cortex-A9 programmer's model
 - Instruction sets
 - Processor modes
 - Register set
 - Co-processors
 - Cortex-A9 functional description
 - Cortex-A9 block diagram
 - Cortex-A9 MPCore
 - Energy efficiency features
 - Pipeline description
 - Register renaming
 - Branch prediction
 - Fast loop mode
 - Performance Monitoring Unit (PMU)



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- NEON technology
- VFPv3 – vector floating point
- L1 memory system
- L1 cache memory
- Write buffer
- Data prefetching
- L2 cache controller (PL310)
- Memory Management Unit (MMU)
- TLB
- Memory access permissions
- Memory ordering
- Memory types in ARMv7
- Cortex-A9 MPCore cache coherency
- Enabling Snoop Control Unit (SCU)
- MESI protocol
- Global Interrupt Controller (GIC)
 - GIC architecture
 - GIC basic initialization
- System debug
 - Embedded cross triggering
 - Debug scheme

➤ **SDMA**

- SDMA block diagram
- SDMA core deep dive
- Scheduler functional description
- Scheduler use case examples
- Context switching
- Burst and peripheral DMA
- Security support
- OnCE & PCU debug states
- SDMA programming model
- Address space
- Hardware reset effect
- Standard boot sequence
- Script loading & context initialization

➤ **IOMux Controller**

- Introduction
- IOMUX features
- Choosing signals and resolving pin conflicts
- Ensuring voltage consistency per module
- Alternate IOMUX views
- Demonstration on IOMUX tool



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- **GPMI & NAND Interface**
 - NAND controller overview
 - General Purpose Media Interface (GPMI)
 - GPMI NAND mode
 - Multiple NAND support
 - Hardware BCH interface
 - 40-bit correcting ECC accelerator (BCH)
 - BCH limitations and assumptions
 - NAND bottlenecks

- **1G Ethernet (optional)**
 - MAC-NET features
 - MAC-NET block diagram
 - IP protocol performance optimization features
 - IEEE 1588 features
 - Media independent interface
 - Ethernet clock generation

- **MIPI Display & Sensor Interfaces (optional)**
 - MIPI DSI
 - MIPI DBI
 - MIPI CSI-2
 - MIPI HSI

- **HDMI (optional)**
 - General features
 - Block diagram and supported formats
 - Audio DMA interface
 - HDCP (secured HDMI)
 - CEC hardware engine



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Day #3

❖ i.MX6 Boot, Security & Multimedia

➤ i.MX6 Boot

- System Boot overview
- Boot modes and boot sources
- Boot mode pin settings
- Boot from fuses
- Serial downloader
- Internal boot
- Boot security settings
- GPIO override pads
- Multi-core Boot flow
- Boot block activation
- Enabling MMU and caches
- Program image
- High Assurance Boot (HAB)
- Secure Boot components
- Encrypted image support
- USB low power Boot

➤ Security

- i.MX6 security features
- Security subsystem block diagram
- Common security attacks
- TrustZone: CPU secure & non-secure worlds
- Boot ROM
- Cryptographic Acceleration and Assurance Module (CAAM)
- Secure memory
- Algorithm acceleration
- Secure non-volatile storage (SNVS)
- Secure JTAG Controller (SJC)
- Memory & peripheral isolation for TrustZone support

➤ Image Processing Unit (IPU)

- Video sources
- Display sources
- IPU block diagram
- The display port
- Access modes (synchronous/asynchronous)
- Display Interface (DI)
- Display Controller (DC)



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- Display Multi-FIFO Controller (DMFC)
- Image DMA Controller (IDMAC)
- Display Processor (DP)
- Image Converter (IC)
- Image Rotator (IRT)
- Video De-Interlace or Combiner (VDIC)
- Basic combining capabilities
- Off-line combining
- Maximal on-the-fly combining to a single and multi-displays
- IPU programming steps
- Camera Sensor Interface (CSI)
- 16-bit camera support
- MIPI CSI-2
- Control Module (CM)
- Display Content Integrity Checker (DCIC)

➤ **Video Processing Unit (VPU)**

- The multimedia processing chain
- Decoder
- Encoder
- Multi-streams
- On-the-fly transcoding
- Full duplex HW Codec
- Codec licensing
- VPU architecture overview (BIT processor)
- Normal and Low power modes
- VPU initialization (Boot)
- VPU-IPU interface
- Bandwidth for typical worse case
- VPU driver API
- VPU software structure

➤ **Graphics Processing Unit (GPU)**

- Graphics processing units (Vivante GC2000, GC320, GC355, GC880)
- Graphics processing advantages
- Composition engine GPU
- OpenVG vector graphics processor
- OpenGL ES 3D engine
- GPU architecture
- GPU SDK
- GPU application development
- OpenCL



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