Intel® FPGA Technical Training

Quartus Prime Pro for Vivado Users

Course Description

This course provides all theoretical and practical know-how to design programmable devices of Intel with Quartus Prime Pro design software.

The course combines 50% theory with 50% practical work in every meeting. The practical labs cover all the theory.

The course starts with an overview of the Quartus Prime Pro design software features versus Vivado, Quartus Prime Pro projects types and management, design methodology, and using IP cores from the IP catalog. Platform Designer, state machine editor, memory editor, Intel SDK for OpenCL, and DSP Builder are also introduced in high level.

The course continues with Quartus Prime Pro compilation flow, working with messages, viewing compilation reports, RTL and technology views, state machine viewer, and how to use the chip planner tool.

The course also touches upon synthesis and Place & Route settings and assignment editor, optimizations, and various advisors.

The course ends with I/O planning with the pin planner, with the Interface Planner, programming and configuration of FPGA/CPLD.

Course Duration

2 days

Goals

1. Create a new Quartus Prime project
2. Choose supported design entry methods
3. Compile a design into a programmable logic device
4. Locate resulting compilation information
5. Create design constraints (assignments & settings)
6. Manage I/O assignments
7. Prepare for programming/configuring a programmable logic device

Intended Users

Hardware engineers who use Xilinx FPGAs with the Vivado software, and would like to be specialized with Intel FPGAs and Quartus Prime software

Previous Knowledge

VHDL/Verilog beginners and advanced users who are new to Intel FPGAs.

Course Material

1. Synthesizer and Place & Route: Quartus Prime Pro
2. Course book (including labs)

Table of Contents

Day #1

- **Solutions Portfolio Comparison**
  - CPLD: MAX vs CoolRunner-II
  - Low Cost FPGA: Cyclone vs Spartna7
  - Mid-Range FPGA: Arria vs Kintex
  - High Performance FPGA: Stratix vs Virtex

- **Introduction to Quartus Prime Pro Software**
  - Lite Edition, Standard Edition and Pro Edition
  - Migration paths
  - Software licensing
  - Quartus vs Vivado software comparison
  - Quartus Prime Pro design software features
  - Quartus Prime Pro default operating environment
  - Tips and tricks advisor
  - Built in help system
  - Tasks window
  - TCL and command line help

- **Quartus Prime Pro Projects**
  - Project creation and project types
  - Intel FPGA design store
  - EDA tool settings
  - Quartus Prime Pro project files and folders vs Xilinx
  - Constraint files & assignment priority
  - Project management (archive, restore, copy, revisions, clean)
  - IP management tools

❖ **Lab #1: Create a Project in Quartus Prime Pro**

- **Design Methodology**
  - Typical PLD design flow
  - Design entry methods
  - Design entry file types supported
  - Verilog & VHDL support
  - Intel FPGA IP cores (Xilinx LogiCORE IP)
  - IP base suite
  - IP catalog
  - Creating an IP variation with the IP parameter editor
  - Methods for editing existing IP parameters
  - System design entry with Platform Designer (Xilinx IP Integrator)
  - State machine editor
  - Memory editor
  - DSP Builder standard/advanced blocksets (Xilinx System Generator)
  - Open Computing Language (OpenCL) (Xilinx SDAccel Development Environment)
  - Synthesis and P&R
  - Programmer

❖ **Lab #2: Use IPs from the IP Catalog and the Memory Editor**

- **RTL Coding Guidelines for Quartus Prime Pro Integrated Synthesis**
  - Synthesis directives and attributes
  - Fixed output registers
  - RAM inference
  - Latch inference
  - Combinational loops
  - Finite state machine coding styles

- **Lab #3: Use Synthesis Attributes to Affect Quartus Prime Pro Synthesis Results**

Day #2

- **Quartus Prime Compilation**
  - Quartus Prime Pro full compilation flow
  - Quartus Prime Pro synthesis
  - Intel and Xilinx flow stages
  - What is the fitter?
  - Fitter stages (Plan, Early Place, Place, Route, Retime, Finalize)
  - Processing options
  - Compilation dashboard
  - Notification center
  - Reducing compile times
  - Rapid Recompilation (Xilinx ECO)
  - Messages window
  - Viewing compilation results
  - Netlist viewers
  - State machine viewer
  - Chip planner (Xilinx floorplanning)
  - LogicLock regions (Xilinx pblocks)
  - Cross-probing from/to Chip Planner
  - Why did I receive undesired results?

❖ **Lab #4: Compile a Project in Quartus Prime Pro, Locate Information in the Compilation Report, and explore cross-probing capabilities by viewing logic in various windows**

- **Settings & Assignments**
  - Synthesis and fitting control
  - Setting dialog box
  - Device settings
  - Consolidated compiler optimization settings (synthesis & fitter)
  - Assignments (Xilinx .xdc file)
  - Assignment editor features
  - Creating assignments: cross-probing
  - Creating assignments: Assignment Editor
  - Assignment groups
  - Updating .qsf file

- Assignment Tcl commands
- Export assignments
- Advisors

❖ **Lab #5: Create a New Revision and Make Design Constraints using the Assignment Editor**

- **I/O Planning**
  - I/O planning need
  - Creating I/O related assignments
  - Pin planner tool (Xilinx I/O Planning)
  - Assigning pin locations using pin planner
  - Pin Legend and Pin Planner views
  - More Pin Planner features
  - Pin planner tasks & report windows
  - Reserved and unused I/O pins
  - Show Fitter placements
  - Back-annotation
  - Verifying I/O assignments
  - I/O rules checked
  - I/O assignment analysis output
  - Validating I/O pin-put
  - I/O planning with the Interface Planner (Xilinx Memory Bank/Byte Planner)
  - Import/export via CSV
  - .qsf editing and scripting
  - Global pin settings
  - Using synthesis attributes in HDL

❖ **Lab #6: Assign I/O Pins and Perform I/O Assignment Analysis, Back Annotate Pin Assignments to lock placement, and Use the Interface Planner tool to create I/O assignments for a design**

- **Programming & Configuration**
  - Programming files (sof, pof, jam/jbc, jic)
  - Programming file conversion
  - Quartus Prime pro programmer (Xilinx Hardware Manager)