# Designing with STM32H7 Family

## Course Description

Designing with STM32H7 Family is a 3 days ST official course.

The course provides all necessary theoretical and practical know-how for start developing platforms based on STM32H7xx families with STMCube.

The course begins with an introduction to STM32 microcontroller family's roadmap and focuses on Cortex-M7 architecture.

The course continues with an in-depth study of the memory organization, bus architecture, reset and clock controller, interrupts handling, low power modes, hardware semaphore, MDMA, security, and most of the SoC peripherals such as clocks, reset, embedded Flash, FMC, NVIC, EXTI, ADC, USART, DAC, SPI, USB, DMA, crypto processor, Hash processor, RNG and debug.

The course also employs hardware and software design tools, and combines 50% theory with 50% practical work in every meeting.

## Course Duration

3 days

## Goals

1. Become familiar with STM32H7 families
2. Become familiar with ARM Cortex-M7 architecture
3. Understand the bus and memory topology to get the best performance
4. Become familiar with STM32H7 peripherals
5. Become familiar with hardware and software design tools
6. Build a new project using the STMCube
7. Work with Firmware libraries

## Target Audience

Software engineers who would like start developing with STM32H7xxx microcontrollers

# Prerequisites

- Computer architecture background
- Experience in C programming
- Experience in developing embedded systems

# Course Material

- STMCube
- ST Eval board: STM32H743I-EVAL
- Course book (including labs)

# Agenda

## Day #1

- **STM32H7 Series Overview**
  - STM32H7 block diagram
  - STM32H7 product series

- **STM32H7 System Architecture**
  - System architecture overview
  - AXI and AHB bus matrices
  - TCM buses
  - Bus bridges
  - Inter-domain buses
  - Cortex-M7 busses (AXIM, ITCM, DTCM, AHBS, AHBP)
  - Bus master peripherals
  - AXIM interconnect (NIC-400)

- **STM32H7 Memory Organization**
  - Memory map
  - Embedded SRAM (D1, D2, D3 domains, TCMs)
  - ECC
  - Embedded Flash
  - Boot configuration
  - Embedded bootloader

- **STM32H7 Embedded Flash**
  - Main features supported
  - Flash block diagram
  - Protection mechanism
  - Flash programming/erase/read operations
  - Flash parallel operations
  - ECC and CRC
  - Flash bank and register swapping
  - Clock and reset management
  - Flash option bytes
  - Low power modes
  - interrupts

- **STM32H7 Reset & Clock Control (RCC)**
  - Main features supported
  - RCC block diagram
  - Which sources can generate reset?
  - Power-on/off reset
  - System reset
  - Local reset
  - Identifying reset source
  - Low power mode security reset
  - Backup domain reset
  - Power-on wakeup sequence
  - Boot from pin reset
  - Boot from system standby
  - Clock generators (HIS, HSE, LSE, LSI, CSI, HSI48)
  - Clock security system (CSS)
  - Clock output generation
  - PLLs
  - System clock selection & generation
  - Clock generators behavior in stop and standby modes
  - Peripheral allocation and clock gating control
  - CPU and bus matrix clock gating control
  - RCC interrupts

# Day #2

- **STM32H7 Hardware Semaphore**
  - The race for atomicity
  - HSEM main features
  - HSEM block diagram
  - HSEM lock procedures
  - HSEM clear procedures
  - HSEM interrupts
  - AHB bus master ID verification

- **STM32H7 Master DMA Controller (MDMA)**
  - MDMA main features
  - MDMA block diagram
  - MDMA transactions over AXI/AHB
  - MDMA channel
  - Pointer update
  - MDMA buffer transfer
  - Request arbitration
  - FIFO
  - Block transfer
  - Block repeat and linked list modes
  - MDMA transfer completion and suspension
  - Error management
  - MDMA interrupts

- **STM32H7 DMA & BDMA Controllers**
  - DMA main features
  - DMA block diagram
  - DMA transactions
  - DMA request mapping
  - Arbiter
  - DMA streams
  - Transfer modes
  - Pointer incrementation
  - Circular and double buffer modes
  - Programmable data width
  - Single and burst transfers
  - FIFO
  - DMA transfer completion and suspension

- Flow controller
- Error management
- DMA interrupts
- BDMA main features
- BDMA block diagram
- BDMA transfers
- BDMA arbitration
- BDMA channels
- BDMA error management
- BDMA interrupts

- **STM32H7 DMA Request Multiplexer (DMAMUX)**
  - DMAMUX main features
  - DMAMUX block diagram
  - DMAMUX channels
  - DMAMUX request line multiplexer
  - DMAMUX request generator
  - DMAMUX interrupts

- **STM32H7 NVIC and EXTI**
  - NVIC features
  - SysTick calibration value register
  - Interrupt and exception vectors
  - EXTI main features
  - EXTI block diagram
  - EXTI configurable event input CPU wakeup
  - EXTI configurable event input ANY wakeup
  - EXTI direct event input CPU wakeup
  - EXTI direct event input ANY wakeup
  - EXTI event input mapping
  - EXTI CPU event and interrupt procedures
  - EXTI software interrupt/event trigger procedure

- **STM32H7 Flexible Memory Controller (FMC)**
  - FMC features
  - FMC block diagram
  - AHB and AXI interfaces
  - Supported memories and transactions
  - External device address mapping
  - NOR Flash/PSRAM controller
  - Synchronous and asynchronous transactions

- NAND Flash controller
- NAND Flash supported memories and transactions
- NAND Flash operations
- NAND Flash prewait feature
- ECC in NAND Flash
- SDRAM controller
- SDRAM initialization
- SDRAM controller write cycle
- SDRAM controller read cycle
- Row and bank boundary management
- SDRAM controller refresh cycle
- Low power modes (self-refresh, power down)

- **STM32H7 Secure Memory Management**
  - Flash protections
  - Secure access mode
  - Root secure services
  - Secure user software

- **STM32H7 True Random Number Generator (RNG)**
  - RNG main features
  - RNG block diagram
  - Random number generation
  - RNG initialization
  - Normal operations
  - Low power operations
  - RNG clocking
  - Error management
  - RNG low power usage
  - RNG interrupts
  - RNG processing time
  - Entropy source validation

- **STM32H7 Cryptographic Processor (CRYP)**
  - CRYP main features
  - CRYP block diagram
  - CRYP DES/TDES cryptographic core
  - CRYP AES cryptographic core
  - CRYP stealing and data padding
  - Suspend/resume operations
  - ECB, CBC chaining modes

- AES counter mode
- CRYP data registers and data swapping
- DMA interface
- CRYP interrupts
- CRYP processing time

- **STM32H7 Hash Processor (HASH)**
  - HASH main features
  - HASH block diagram
  - Hash algorithms
  - Message data feeding
  - Message digest computing
  - Message padding
  - HMAC processing
  - Context swapping
  - HASH DMA interface
  - HASH interrupts
  - HASH processing time

## Day #3

- **STM32H7 ADC**
  - ADC main features
  - ADC block diagram
  - Dual clock domain architecture
  - BOOST bit control
  - ADC 1/2/3 connectivity
  - Deep power down mode & voltage regulator
  - Single ended and differential input channels
  - Calibration
  - On-off control
  - Channel selection
  - Conversion modes
  - Stopping an ongoing conversion
  - Conversion on external trigger
  - Injected channel management
  - Discontinuous mode
  - Fast conversion mode
  - Data management
  - Dynamic low power features

- Analog window watchdog
- Oversampler
- Dual ADC modes
- Temperature sensor
- Monitoring the internal voltage reference
- ADC interrupts

- **STM32H7 DAC**
  - DAC main features
  - DAC block diagram
  - DAC data format
  - DAC conversion
  - DAC output voltage
  - DAC trigger selection
  - DMA requests
  - Noise generation
  - Triangle wave generation
  - DAC channel modes
  - DAC channel buffer calibration
  - Dual DAC channel conversion
  - DAC interrupts

- **STM32H7 Independent Watchdog (IWDG)**
  - IWDG features
  - IWDG block diagram
  - Window option
  - Low power freeze
  - Register access protection
  - Debug mode

- **STM32H7 Window Watchdog (WWDG)**
  - WWDG features
  - WWDG block diagram
  - Enabling the watchdog
  - Controlling the downcounter
  - Advanced watchdog interrupt feature
  - How to program the watchdog timeout
  - Debug mode

- **Universal Synchronous Asynchronous Receiver Transmitter (USART)**
  - USART features
  - Extended capability
  - USART block diagram
  - USART character description
  - USART FIFOs and thresholds
  - USART transmitter & receiver
  - USART baud rate generation
  - USART auto baud rate detection
  - USART multiprocessor communication
  - USART Modbus communication
  - USART parity control
  - USART LIN mode
  - USART synchronous mode
  - USART smartcard mode
  - USART IrDA SIR
  - USART and DMA
  - RS232 and RS485 support
  - USART low power management
  - USART interrupts

- **Serial Peripheral Interface (SPI) and I2S**
  - SPI features
  - SPI block diagram
  - Communications between one master and one slave
  - Standard multi-slave communication
  - Multi-master communication
  - Slave select pin management
  - Communication formats
  - SPI data transmission and reception procedures
  - Data packing
  - Disabling SPI
  - Communication using DMA
  - SPI modes and control
  - CRC computation
  - Low power mode management
  - SPI wakeup and interrupts
  - I2S main features
  - Pin sharing with SPI function
  - Slave and master modes

- Supported audio protocols
- Internal FIFOs
- Frame error detection
- DMA interface
- I2S wakeup and interrupts

- **USB 2.0 On-The-Go High Speed (OTG HS)**
  - Main features
  - Host mode features
  - Peripheral-mode features
  - OTG block diagram
  - OTG dual role device
  - USB peripheral
  - USB host
  - SOF trigger
  - OTG low power modes
  - USB data FIFOs
  - OTG_HS interrupts

- **Ethernet MAC 10/100**
  - Main features
  - Ethernet block diagram
  - DMA features
  - AHB master interface
  - AHB slave interface
  - DMA controller
  - MTL
  - MAC
  - Double VLAN processing
  - Packet filtering
  - IEEE 1588 timestamps
  - TCP segmentation offload
  - Loopback
  - Flow control
  - Checksum offload engine
  - MAC management counters
  - MAC interrupts
  - PHY interfaces
  - Ethernet low-power modes
  - Ethernet interrupts
  - Ethernet programming model

- Descriptors

- **Debug**
  - Debug main features
  - Debug infrastructure block diagram
  - Clock domains and reset
  - Debug Access Port (DAP)
  - Access ports
  - System ROM tables
  - Global timestamp generator
  - System cross trigger interface
  - Cross trigger matrix
  - Trace port interface unit
  - Trace bus funnel
  - Embedded trace FIFO
  - Serial wire output
  - Serial wire output trace funnel